Power Roadmap
POWER8
POWER7 Portfolio

Virtualization & Mgmt.

PowerVM

IBM Systems Director

Power

AIX

Linux

Power 710+/730+

Power 720+/740+

Power 750+

Power 760+

Power 770+

Power 780+

Power 795

PowerLinux

7R1 / 7R2 / 7R4

7R1 / 7R2 / 7R4

PureSystems

p460+

p270+

p260+

p24L

PureApps

PureData

PureFlex
Processor Directions

More Cores
4th Gen SMT
Encryption Logic
CAPI
PCIe Acceleration
Transactional memory
Enhanced Caches

8 Cores
3rd Gen SMT
L3+ On Chip

Dual Cores
Dual Threads
External L3

POWER4/4+
180 / 130 nm

POWER5/5+
130 / 90 nm

POWER6/6+
65 nm

POWER7/7+
45/32 nm

POWER8
22 nm
POWER8 Vision

Leadership Performance

• Increase core throughput at single thread, SMT2, SMT4, and SMT8 level
• Large step in per socket performance
• Enable more robust multi-socket scaling

System Innovation

• Higher capacity cache hierarchy and highly threaded processor
• Enhanced memory bandwidth, capacity, and expansion
• Dynamic code optimization
• Hardware-accelerated virtual memory management

Open System Innovation

• Coherent Accelerator Processor Interface (CAPI)
• Agnostic Memory interface
• Open system software

Optimize Analytics & Big Data

Enhance Cloud Efficiency

Enable Open Innovation on POWER
POWER8 Architecture
POWER8 Core

Execution Improvement vs. POWER7

SMT4 → SMT8
• 8 dispatch
• 10 issue
• 16 execution pipes:
  • 2 FXU, 2 LSU, 2 LU, 4 FPU, 2 VMX, 1 Crypto, 1 DFU, 1 CR, 1 BR
• Larger Issue queues (4 x 16-entry)
• Larger global completion, Load/Store reorder
• Improved branch prediction
• Improved unaligned storage access

Larger Caching Structures vs. POWER7
• 2x L1 data cache (64 KB)
• 2x outstanding data cache misses
• 4x translation Cache

Wider Load/Store
• 32B → 64B L2 to L1 data bus
• 2x data cache to execution dataflow

Enhanced Prefetch
• Instruction speculation awareness
• Data prefetch depth awareness
• Adaptive bandwidth awareness
• Topology awareness

Core Performance vs. POWER7

~1.6x Single Thread
~2x Max SMT
POWER8 Chip Packaging

Technology
- 22nm SOI, eDRAM, 15 ML 650mm2

Caches
- 512 KB SRAM L2 / core
- 96 MB eDRAM shared L3
- Up to 128 MB eDRAM L4 (off-chip)

Memory
- Up to 230 GB/s sustained bandwidth

Bus Interfaces
- Durable open memory attach interface
- Integrated PCIe Gen3
- SMP Interconnect
- CAPI (Coherent Accelerator Processor Interface)

Cores
- 12 cores (SMT8)
- 8 dispatch, 10 issue, 16 exec pipe
- 2X internal data flows/queues
- Enhanced prefetching
- 64K data cache, 32K instruction cache

Accelerators
- Crypto & memory expansion
- Transactional Memory
- VMM assist
- Data Move / VM Mobility

Energy Management
- On-chip Power Management Micro-controller
- Integrated Per-core VRM
- Critical Path Monitors
POWER8 on Chip Caches

- L2: 512 KB 8 way per core
- L3: 96 MB (12 x 8 MB 8 way Bank)
- “NUCA” Cache policy (Non-Uniform Cache Architecture)
  - Scalable bandwidth and latency
  - Migrate “Hot” lines to local L2, then local L3 (replicate L2 contained footprint)
- Chip Interconnect: 150 GB/sec x 12 segments per direction = 3.6 TB/sec
POWER8 Memory Buffer Chip

Intelligence Moved into Memory
- Scheduling logic, caching structures
- Energy Mgmt, RAS decision point
  - Formerly on Processor
  - Moved to Memory Buffer

Processor Interface
- 9.6 GB/s high speed interface
- More robust RAS
  - “On-the-fly” lane isolation/repair
- Extensible for innovation build-out

Performance Value
- End-to-end fastpath and data retry (latency)
- Cache → latency/bandwidth, partial updates
- Cache → write scheduling, prefetch, energy
- 22nm SOI for optimal performance / energy
- 15 metal levels (latency, bandwidth)
## Transactional Memory

### Definition
- Technique that allows a group of instructions including updates to memory image to execute speculatively and atomically. This group of instructions is called a transaction.

### Value
- Reducing programming development
- Reducing customer cost (higher SLA / fewer images and higher scalability
- Improving performance of legacy software with large sequential components

### Power8 Support
- New instructions mark beginning and end of transaction
  - Hardware ensures region is performed atomically using speculation
- Speculation recovery performed in hardware, both registers and memory
- “Flattened” Nesting
  - Hardware tracks nesting of transactions
  - Treats them all as a single large transaction

### Application-level instruction interface
- Transaction Begin/End Instructions
- Explicit abort
- Diagnostic register - Transaction Exception and Summary Register
  - Indicates cause of transaction failure
POWER8 Integrated PCI Gen 3

Native PCIe Gen 3 Support
- Direct processor integration
- Replaces proprietary GX/Bridge
- Low latency
- Gen3 x16 bandwidth (16 Gb/s)

Transport Layer for CAPI Protocol
- Coherently Attach Devices connect to processor via PCIe
- Protocol encapsulated in PCIe

POWER7

I/O Bridge

PCI Devices

POWER8

PCIe G3

PCI Device
POWER8 CAPI (Coherent Accelerator Processor Interface)

Virtual Addressing
- Accelerator can work with same memory addresses that the processors use
- Pointers de-referenced same as the host application
- Removes OS & device driver overhead

Hardware Managed Cache Coherence
- Enables the accelerator to participate in “Locks” as a normal thread
  Lowers Latency over IO communication model

Customizable Hardware Application Accelerator
- Specific system SW, middleware, or user application
- Written to durable interface provided by PSL

Custom Hardware Application
- FPGA or ASIC

Processor Service Layer (PSL)
- Present robust, durable interfaces to applications
- Offload complexity / content from CAPP

PCle Gen 3
Transport for encapsulated messages

POWER8
Coherence Bus
CAPP
Socket Performance
Beta Program

Client Experience
- Handons testing with POWER8 hardware

Advocate/ESP support team
- Extended team will monitor client testing progress against test matrix & collect feedback/experience

ESP Execution
- Wkly Interlock Mtg for extended ESP team

Program to include support for..
- AIX
- IBM i
- Linux / Powerlinux
- Simplify PowerVM

Client Requirements
- Perform meaning testing
- Weekly calls
- Some minimal education

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