Introducing the newest members of the zEnterprise System family
The zEnterprise EC12 and zEnterprise BladeCenter Extension Model 003

IBM zEnterprise EC12 (zEC12)
• zEC12 has the industry’s fastest superscalar chip with each core at 5.5 GHz
• New innovation to drive availability with IBM zAware and Flash Express
• Optimized for the corporate data serving environment
• Hardware functions boost software performance for Java™, PL/I, DB2®

IBM zEnterprise Unified Resource Manager and zEnterprise BladeCenter Extension (zBX) Mod 003
• Supports the new zEC12 platform
• Hosts PS701 and HX5 blades
• Provides workload-awareness resource optimization
• Enhancements to System Director support zBX
• System z will continue to expand hybrid computing

Plus more flexibility and function by connecting to IDAA
• IBM DB2 Analytics Accelerator (IDAA) allows deployment of business analytics on the same platform as operational applications
• Analytics and OLTP can be run as the same workload
IBM System z

zEnterprise EC12 is the core of next generation System z

**zEC12**

*Machine Type: 2827*

*Models: H20, H43, H66, H89, HA1*

- Advanced Technology 5.5 GHz processor chip for performance boost for all workloads
  - Over **78,000 MIPS** for large scale consolidation
  - **Larger cache** for data serving
- Processor chip optimized for software performance
  - Advanced performance functions exploited by **Java, PL/I, compilers, DB2** and more
- Innovation to drive availability to superior levels
  - **IBM zAware** with out-of-band analytics provide point in time snapshot of the current state of your business and can help you improve availability
  - **FLASH Express and pageable large pages** to drive availability and performance for critical workloads
- Security and reliability are in our DNA
  - High speed **cryptography integrated as part of the chip**
  - Enhanced support for applications requiring data encryption, cryptographic keys and digital signing with new **Crypto Express4S**
  - PR/SM designed for **EAL5+ certification**

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Processor chip optimized for software performance

Exploited by Java, PL/I, compilers, DB2, more

- **Our leadership in microprocessor design supports a boost in performance for all workloads**
  - Second generation out of order design
  - Multi-level branch prediction supports complex workloads

- **Larger caches to optimize data serving environments**
  - Almost 2x on chip and 2x additional on book

- **New hardware functions optimized for software performance**
  - *Transactional Execution Facility* for parallelism and scalability
  - *Runtime Instrumentation Facility* is intended to help reduce Java overhead
  - *2 GB page frames* are intended to offer performance improvements for DB2 buffer pools and Java heaps
  - Up to **30% improvement in IMS throughput** due to faster CPU and cache, compilers, and more
  - New IBM Enterprise PL/I compiler is planned to exploit and get a performance boost from *decimal format conversions facility*

**Excellent Results:**

- Up to **45%** improvement for Java workloads
- Up to **27%** improvement in CPU intensive int & float C/C++ applications
- Up to **30%** improvement in throughput for DB2 for z/OS operational analytics
- More than **30%** improvement in throughput for SAP workloads

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1 Based on preliminary internal measurements and projections
2 Ameasured by the IBM 9700 Solution Integration Center. The measured operational BI workload consists of 56 concurrent users executing a fixed set of 160,860 Cognos reports. Compared DB2 v10 workload running on IBM's z196 w/10 processors to an zEC12 w/10 processors
IBM System z: Design Comparison for High End Systems

* Servers exploit a subset of its designed I/O capability
** Up to 1 TB per LPAR
PCI – Processor Capacity Index

Balanced System CPU, nWay, Memory, I/O Bandwidth*

- System I/O Bandwidth
  - 384 GB/Sec*
  - 288 GB/sec*
  - 172.8 GB/sec*
  - 96 GB/sec
  - 24 GB/sec
  - 16 GB/sec
  - 64 GB/sec
  - 256 GB
  - 512 GB
  - 1.5 TB**
  - 3 TB**
  - 1202 PCI for 1-way
  - 1514

80-way
64-way
54-way
64-way
101-way Processors

zEC12
z196
z10 EC
z9 EC
zSeries 990
zSeries 900

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## Extending System z Availability with Flash Express and IBM zAware

<table>
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<th>Operations Availability</th>
<th>Business Application Availability</th>
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<td>Availability</td>
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<td>Hardware checks</td>
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<tr>
<td>Parallel Sysplex</td>
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</tr>
</tbody>
</table>

- Designed to Prevent Hard Failures
- Designed to Improve System SW Availability
- Designed to improve Continuous Operations
- Designed to Improve Business Availability
Synergy with zEC12 Operating Systems

**z/OS**
- Java exploitation of Transactional Execution for increased parallelism and scalability
- Enhanced security support for digital signatures
- Faster problem determination with IBM zAware for improved availability
- Improve availability and performance with Flash Express
- 2 GB page support
- Simpler Specialty Engine (zIIP) exploitation
- z/OS v1.13 exploitation of new hardware
- z/OS health checks for SAN for new channel path selection
- Plus over 4,100 applications enabled on z/OS

**Linux on System z**
- Improved consolidation ratio through new capacity performance
- Improved I/O performance using High Performance FICON (zHPF)
- Application and Linux optimization enabled by full exploitation of zArchitecture extensions
- Optimized system setup via Linux health checker
- FCP end-to-end data integrity checking for applications and storage subsystems
- Plus over 3,000 applications on System z

**z/TPF**
- Support for 86 CPUs
- Hardware exploitation for performance improvements

**z/VM**
- z/VM Compatibility support
- Guest exploitation support for new OSA and encryption technology
- Simplified data exchange of virtual Linux servers using z/VM software
- Improved I/O performance using High Performance FICON (zHPF) for guest exploitation
- AND with blades on the zBX there are even more options with applications on AIX, Linux on System x or Microsoft Windows

**z/VSE**
- 64-bit addressing with z/VSE V5.1
- Strong interoperability with Linux on System z
- New CICS functionality (CICS Explorer)
IBM zEnterprise System - 2012

IBM zEnterprise EC12 (zEC12)  IBM zEnterprise BladeCenter Extension (zBX Model 003)

IBM zEnterprise Unified Resource Manager

Note: Covers for zBX. New zBX Model 003s will be shipped with new design covers with a blue stripe. zBX Model 002s upgraded to Model 003s will retain existing design covers
System z Servers Continue to Scale with zEC12

Each new range continues to deliver:

- New function
- Unprecedented capacity to meet consolidation needs
- Improved efficiency to further reduce energy consumption
- Continues to delivering flexible and simplified on demand capacity
- A mainframe that goes beyond the traditional paradigm

PCI - Processor Capacity Index

*z/OS supports up to a 100-way only
zEC12 Continues the CMOS Mainframe Heritage Begun in 1994

- 189 nm SOI
- 16 Cores
- Full 64-bit z/Architecture

- 130 nm SOI
- 32 Cores
- Superscalar Modular SMP

- 90 nm SOI
- 54 Cores
- System level scaling

- 65 nm SOI
- 64 Cores
- High-freq core
- 3-level cache
- OOO core
- eDRAM cache
- RAIM memory
- zBX integration

- 45 nm SOI
- 80 Cores
- OOO and eDRAM cache improvements
- PCIe Flash
- Arch extensions for scaling
# zEnterprise EC12 Functions and Features

*(GA Driver Level 12K – September, 2012)*

## zEnterprise EC12 Functions and Features

<table>
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<th>Feature</th>
<th>Description</th>
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<td>Five hardware models</td>
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<tr>
<td>Six core 32nm PU chip</td>
<td></td>
</tr>
<tr>
<td>Up to 101 processors configurable as CPs, zAAPs, zIIPs, IFLs, ICFs, or optional SAPs</td>
<td></td>
</tr>
<tr>
<td>Increased capacity processor (1.25 x z196)</td>
<td></td>
</tr>
<tr>
<td>Up to 20 sub capacity CPs at capacity settings 4, 5, or 6</td>
<td></td>
</tr>
<tr>
<td>z/Architecture Enhancements including 2 GB Pages, Transactional Execution and Runtime Instrumentation</td>
<td></td>
</tr>
<tr>
<td>2nd Generation out-of order design</td>
<td></td>
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<tr>
<td>Enhanced processor cache design</td>
<td></td>
</tr>
<tr>
<td>Dedicated data compression and crypto coprocessor on each PU</td>
<td></td>
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<tr>
<td>Up to 3 TB of Redundant Array of Independent Memory (RAIM)</td>
<td></td>
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<tr>
<td>Flask Express and pagable large page support</td>
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<tr>
<td>Crypto Express4S and Cryptographic enhancements</td>
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<tr>
<td>New Channel path selection algorithms</td>
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<tr>
<td>OSA-Express 4S 1000BASE-T</td>
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<td>CFCC Level 18</td>
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<td>IBM zAware</td>
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<tr>
<td>On Demand enhancements</td>
<td></td>
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<td>Non-Raised floor option for Air Cooled System only with overhead I/O and power cabling options</td>
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</tr>
<tr>
<td>Raised floor option for Air and Water Cooled System with overhead I/O and power cabling options</td>
<td></td>
</tr>
<tr>
<td>New ‘radiator’ design for Air Cooled System</td>
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<tr>
<td>Optional water cooling with Exhaust Air Heat Exchanger &amp; air backup</td>
<td></td>
</tr>
<tr>
<td>Cycle Steering for Power Save and back-up for radiator and water cooled systems</td>
<td></td>
</tr>
<tr>
<td>Optional High Voltage DC power</td>
<td></td>
</tr>
<tr>
<td>Static Power Save Mode</td>
<td></td>
</tr>
<tr>
<td>Optional overhead Power and I/O cabling</td>
<td></td>
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<tr>
<td>NTP Broadband Authentication</td>
<td></td>
</tr>
<tr>
<td>zBX Model 003 and Unified Resource Manager</td>
<td></td>
</tr>
</tbody>
</table>
zEC12 New Build Radiator-based Air cooled – Under the covers (Model H89 and HA1) Front view

- Overhead Power Cables (option)
- Internal Batteries (option)
- Power Supplies
- 2 x Support Elements
- PCIe I/O drawers (Maximum 5 for zEC12)

- Processor Books with Flexible Support Processors (FSPs), PCIe and HCA I/O fanouts
- PCIe I/O interconnect cables and Ethernet cables FSP cage controller cards
- Radiator with N+1 pumps, blowers and motors
- Overhead I/O feature is a co-req for overhead power option
- Optional FICON LX Fiber Quick Connect (FQC) not shown
zEC12 Water cooled (Upgraded from a z196) - Under the covers (Model H89 or HA1) Front view

- Internal Batteries (optional)
- Power Supplies
- Support Elements
- I/O cage Carried Forward
- PCIe I/O drawer
- Processor Books with Flexible Support Processors (FSPs), PCIe and HCA I/O fanouts
- PCIe I/O interconnect cables and Ethernet cables FSP cage controller cards
- N+1 Water Cooling Units
zEC12 Architecture Extensions

• Transactional Execution (aka Transactional Memory)
  – Software-defined sequence treated by hardware as atomic “transaction”
  – Enables significantly more efficient software
    • Highly-parallelized applications
    • Speculative code generation
    • Lock elision
  – Designed for exploitation by Java; longer-term opportunity for DB2, z/OS, others

• 2 GB page frames
  – Increased efficiency for DB2 buffer pools, Java heap, other large structures

• Software directives to improve hardware performance
  – Data usage intent improves cache management
  – Branch pre-load improves branch prediction effectiveness
  – Block prefetch moves data closer to processor earlier, reducing access latency

• Decimal format conversions
  – Enable broader exploitation of Decimal Floating Point facility by COBOL programs
zEC12 Architecture Extensions - continued

• Run-time Instrumentation
  – A new hardware facility for managed runtimes
    • Tailored towards Java Runtime Environment (JRE)
    • Dynamic and self-tuning online recompilation
  – Not the same as current CPU Measurement Facility (CPUMF)
    • Both can be run concurrently
  – Allow dynamic optimization on code generation as it is being executed
    • Requires a much lower overhead environment (than current software-only profiling)
    • Provides information on hardware as well as program characteristics
    • enhances JRE decision-making by providing real-time feedback

• Key features
  – A collection buffer capturing a run-time trace till a instruction sample point, providing
    • “how we get here information”, e.g. branch history
    • Value profiling (of GPR) in the context of path traced
  – Meta-data collected for “what happened” information with the sample instruction
    • Cache miss
    • Branch prediction/resolution
  – 3 modes of sampling; by
    • cycle count, instruction count, or explicit indication
zEC12 Out of Order Detail

• Out of order yields significant performance benefit through
  – Re-ordering instruction execution
    • Instructions stall in a pipeline because they are waiting for results from a previous instruction or the execution resource they require is busy
    • In an in-order core, this stalled instruction stalls all later instructions in the code stream
    • In an out-of-order core, later instructions are allowed to execute ahead of the stalled instruction
  – Re-ordering storage accesses
    • Instructions which access storage can stall because they are waiting on results needed to compute storage address
    • In an in-order core, later instructions are stalled
    • In an out-of-order core, later storage-accessing instructions which can compute their storage address are allowed to execute
  – Hiding storage access latency
    • Many instructions access data from storage
    • Storage accesses can miss the L1 and require 10 to 500 additional cycles to retrieve the storage data
    • In an in-order core, later instructions in the code stream are stalled
    • In an out-of-order core, later instructions which are not dependent on this storage data are allowed to execute
Out of Order Execution – z196 Vs zEC12

- In-order core execution:
  - Instructions 1 through 7:
    - L1 miss
  - Time:

- z196 Out-of-order core execution:
  - Instructions 1 through 7:
    - L1 miss
  - Improved overlapping opportunities

- zEC12 Out-of-order core execution:
  - Instructions 1 through 7:
    - L1 miss
  - Improved overlapping opportunities
zEC12 OoO - Improved instruction delivery and execution

- z196 Out-of-order core execution
- Shorter L1 Miss latency
- Faster millicode execution
- Better Instruction Delivery

- Dependency
- Execution
- Storage access
zEC12 Multi-Chip Module (MCM) Packaging

- 96mm x 96mm MCM
  - 102 Glass Ceramic layers
  - 8 chip sites
- 7356 LGA connections
  - 27 and 30 way MCMs
  - Maximum power used by MCM is 1800W

- CMOS 13s chip Technology
  - PU, SC, S chips, 32nm
  - 6 PU chips/MCM – Each up to 6 active cores
    - 23.7 mm x 25.2 mm
    - 2.75 billion transistors/PU chip
    - L1 cache/PU core
      - 64 KB I-cache
      - 96 KB D-cache
    - L2 cache/PU core
      - 1 MB I-cache
      - 1 MB D-cache
    - L3 cache shared by 6 PUs per chip
      - 48 MB
    - 5.5 GHz
  - 2 Storage Control (SC) chip
    - 26.72 mm x 19.67 mm
    - 3.3 billion transistors/SC chip
    - L4 Cache 192 MB per SC chip (384 MB/Book)
    - L4 access to/from other MCMs
  - 4 SEEPROM (S) chips – 1024k each
    - 2 x active and 2 x redundant
    - Product data for MCM, chips and other engineering information
  - Clock Functions – distributed across PU and SC chips
    - Master Time-of-Day (TOD) function is on the SC
System z Cache Topology – z196 vs. zEC12 Comparison

**z196**

- **L1:** 64KI + 128KD
  - 8w DL1, 4w IL1
  - 256B line size
- **L2**
  - Private 1.5MB Inclusive of L1s
  - 12w Set Associative
  - 256B cache line size
- **L3**
  - Shared 24MB Inclusive of L2s
  - 12w Set Associative
  - 256B cache line size
- **L4**
  - 192MB Inclusive
  - 24w Set Associative
  - 256B cache line size

**zEC12**

- **L1:** 64KI + 96KD
  - 8w DL1, 4w IL1
  - 256B line size
- **L2**
  - Private 1MB Inclusive of DL1
  - Private 1MB Inclusive of IL1
- **L3**
  - Shared 48MB Inclusive of L2s
  - 12w Set Associative
  - 256B cache line size
- **L4**
  - 384MB Inclusive
  - 24w Set Associative
  - 256B cache line size
<table>
<thead>
<tr>
<th>z196 MCM</th>
<th>zEC12 MCM</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>MCM</strong></td>
<td><strong>MCM</strong></td>
</tr>
<tr>
<td>–96mm x 96mm in size</td>
<td>–96mm x 96mm in size</td>
</tr>
<tr>
<td>–6 PU chips per MCM</td>
<td>–6 PU chips per MCM</td>
</tr>
<tr>
<td>• Quad core chips with 3 or 4 active cores</td>
<td>• Hex-core chips with 4 to 6 active cores</td>
</tr>
<tr>
<td>• PU Chip size 23.7 mm x 21.5 mm</td>
<td>• PU Chip size 23.7 mm x 25.2 mm</td>
</tr>
<tr>
<td>• 5.2 GHz</td>
<td>• 5.5 GHz</td>
</tr>
<tr>
<td>• Superscalar, OoO execution</td>
<td>• Superscalar, OoO enhanced</td>
</tr>
<tr>
<td>• L1: 64 KB I / 128 KB D private/core</td>
<td>• L1: 64 KB I / 96 KB D private/core</td>
</tr>
<tr>
<td>• L2: 1.5 MB I+D private/core</td>
<td>• L2: 1 MB I / 1 MB D private/core</td>
</tr>
<tr>
<td>• L3: 24 MB/chip – shared</td>
<td>• L3: 48 MB/chip - shared</td>
</tr>
<tr>
<td>–2 SC chips per MCM</td>
<td>–2 SC chips per MCM</td>
</tr>
<tr>
<td>• L4: 2 x 96 MB = 192 MB L4 per book</td>
<td>• L4: 2 x 192 MB = 384 MB L4 per book</td>
</tr>
<tr>
<td>• SC Chip size 24.5 mm x 20.5 mm</td>
<td>• SC Chip size 28.4 mm x 23.9 mm</td>
</tr>
<tr>
<td>–1800 Watts</td>
<td>–1800 Watts</td>
</tr>
</tbody>
</table>
zEC12 Book Layout

Note: Unlike the z196, zEC12 Books are the same for the Radiator based Air and Water cooled Systems
zEC12 – 4 Book System with Fanouts, OSC and FSP/STP Cards

Oscillator Card
FSP/STP Card
Fanouts
zEC12 Processor Unit allocation/usage

<table>
<thead>
<tr>
<th>Model</th>
<th>Books/PUs</th>
<th>CPs</th>
<th>IFLs ULFLs</th>
<th>zAAPs</th>
<th>zIIPs</th>
<th>ICFs</th>
<th>Std SAPs</th>
<th>Optional SAPs</th>
<th>Std. Spares</th>
<th>Rsvd. PUs</th>
</tr>
</thead>
<tbody>
<tr>
<td>H20</td>
<td>1/27</td>
<td>0-20</td>
<td>0-20 0-19</td>
<td>0-10</td>
<td>0-10</td>
<td>0-20</td>
<td>4</td>
<td>0-4</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>H43</td>
<td>2/54</td>
<td>0-43</td>
<td>0-43 0-42</td>
<td>0-21</td>
<td>0-21</td>
<td>0-43</td>
<td>8</td>
<td>0-8</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>H66</td>
<td>3/81</td>
<td>0-66</td>
<td>0-66 0-65</td>
<td>0-33</td>
<td>0-33</td>
<td>0-66</td>
<td>12</td>
<td>0-12</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>H89</td>
<td>4/108</td>
<td>0-89</td>
<td>0-89 0-88</td>
<td>0-44</td>
<td>0-44</td>
<td>0-89</td>
<td>16</td>
<td>0-16</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>HA1</td>
<td>4/120</td>
<td>0-101</td>
<td>0-101 0-100</td>
<td>0-50</td>
<td>0-50</td>
<td>0-101</td>
<td>16</td>
<td>0-16</td>
<td>2</td>
<td>1</td>
</tr>
</tbody>
</table>

- zEC12 Models H20 to H89 use books with 27 core MCMs. The Model HA1 has 4 books with 30 core MCMs
  - Each MCM uses PU chips with a combination of 4, 5 and 6 active cores
- The maximum number of logical ICFs or logical CPs supported in a CF LPAR is 16
- **The Reserved PU** is not available for customer purchase
- Concurrent Book Add is available to upgrade from model H20 to model H89

**Notes:**
1. At least one CP, IFL, or ICF must be purchased in every machine
2. One zAAP **and** one zIIP may be purchased for each CP purchased even if CP capacity is “banked”.
3. “ULFL” stands for Unassigned IFL
## zEC12 Purchase Memory Offerings

<table>
<thead>
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<th>Model</th>
<th>Standard Memory GB</th>
<th>Flexible Memory GB</th>
<th>Plan Ahead Memory GB</th>
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<tr>
<td>H20</td>
<td>32 - 704</td>
<td>NA</td>
<td>32-704</td>
</tr>
<tr>
<td>H43</td>
<td>32 - 1392</td>
<td>32 - 704</td>
<td>96 - 1392</td>
</tr>
<tr>
<td>H66</td>
<td>32 - 2272</td>
<td>32 - 1392</td>
<td>64 - 2272</td>
</tr>
<tr>
<td>H89</td>
<td>32 - 3040</td>
<td>32 - 2272</td>
<td>96 - 3040</td>
</tr>
<tr>
<td>HA1</td>
<td>32 - 3040</td>
<td>32 - 2272</td>
<td>96 - 3040</td>
</tr>
</tbody>
</table>

- **Purchase Memory** - Memory available for assignment to LPARs
- **Hardware System Area** – Standard 32 GB outside customer memory for system use
- **Standard Memory** - Provides minimum physical memory required to hold base purchase memory plus 32 GB HSA
- **Flexible Memory** - Provides additional physical memory needed to support activation base customer memory and HSA on a multiple book zEC12 with one book out of service.
- **Plan Ahead Memory** – Provides additional physical memory needed for a concurrent upgrade (LIC CC change only) to a preplanned target customer memory
Introducing Flash Express


Planned availability of z/OS exploitation is December 14, 2012
Introducing Flash Express

- Flash Express is intended to improve System z availability
  - Slash latency delays from paging
    - Flash Memory is much faster than spinning disk
    - Flash Memory is much slower than main memory
    - Flash Memory takes less power than either
  - Designed to eliminate delays from SVC Dump processing

- zEC12 offers optional Flash Express memory cards
  - Supported in PCIe I/O drawer with other PCIe I/O cards
  - Installed in pairs for availability
  - No HCD/IOCP definitions required

- Assign Flash Memory to partitions like main memory
  - Assignment is by memory amount, not by feature
  - Each partition’s Flash Memory is isolated like main memory
  - Dynamically increase the partition maximum amount of Flash
  - Dynamically configure Flash Memory into and out of the partition

Time to Read Data measured in System z Instructions

- Real Memory: (256B line)
  ~100 Instructions

- Flash Memory (4K page)
  ~100K Instructions

- External Disk (4K page)
  ~5,000K Instructions
Relative Access Times for different technologies

- **CPU**: Access time < 20 ns
- **Cache**: Access time < 200 ns
- **Random Access Memory (RAM)**: Access time 5-20 micro sec.
- **Flash Express**: Access time 1-3 ms
- **Solid State Drive (SSD) Storage**: Access time < 10 ms
- **WORM, Tape Library**: Access time in seconds
What Is Flash Express?

• Also referred to as Storage Class Memory (SCM)
• Flash Express is internal storage implemented via NAND Flash SSDs (Solid State Drives) mounted in PCIe Flash Express feature cards
  – Plugs into PCIe I/O drawers in pairs
  – Data security provided on the feature cards
  – A pair provides 1.6 TB of storage
  – A maximum of 4 pairs are supported in a system
• Internal Flash is accessed using the new System z architected EADM (Extended Asynchronous Data Mover) Facility
  – An extension of the ADM architecture used in the past with expanded storage
  – Access is initiated with a Start Subchannel instruction
  – Subchannels used were previously reserved
  – Definition in IOCDS is not required
• The main application of internal Flash in zEC12 is paging store for z/OS
  – Provides advantages in resiliency and speed
  – With pageable large pages being introduced in tandem for exceptional performance
Flash Express Exploitation on zEC12

- Flash Express will be exploited by z/OS
  - z/OS V1.13 Flash Web Deliverable – GA December 14, 2012
    - Pagable Large Pages (1 MB)
  - z/OS V1.13 enabling PTFs for RSM enhancements – 1Q2013
    - Flash Dynamic Reconfiguration
    - Optional PLPA and COMMON Page data sets
  - DB2 for z/OS and JAVA SDK7 SR3 will support pageable Large Pages (SoD*)
  - IBM is working with it’s Linux Distribution partners to include support in future Linux on System z distribution releases
  - IMS* CQS will use pageable Large Pages when IMS runs on zEC12 – Availability targeted for end of 2013

*All statements regarding IBM's future direction and intent are subject to change or withdrawal without notice, and represent goals and objectives only.
Security of Data on Flash Express

- System z internal flash can be used for paging, dumping and .....  
  - It can contain all data, including audited personally identifiable data
- Client data on flash is protected by 128 bit AES Encryption  
  - Done using hardware encryption at the device like IBM’s Disk and Tape encryption
- Key Management is provided based on a Smart Card  
  - Smart Card Reader installed in the Support Element
- End of life Audit is based on access to the Smart Card, not access to the Flash Memory  
  - Secure Cryptographic Erase well understood
Allocating Flash Express

Allocating Flash to a partition

- The initial and maximum amount of Flash Memory available to a particular logical partition is specified at the SE or HMC via a new Flash Memory Allocation panel.

- Can dynamically change maximum amount of Flash Memory available to a logical partition.

- Additional Flash Memory (up to the maximum allowed) can be configured online to a logical partition dynamically at the SE or HMC.
  - For z/OS this can also be done via an operator command.

- Can dynamically configure Flash Memory offline to a logical partition at the SE or HMC.
  - For z/OS this can also be done via an operator command.

- Predefined sub-channels, no IOCDS.
  - Sub-channels are allocated from the .25K reserved in sub-channel set 0.
Flash Express Virtualization

• Full virtualization of physical Flash PCIe cards across partitions, software sees an Abstrated Flash Storage Space…
  – Allows each logical partition to be configured with its own SCM address space
  – Allocate Flash to partitions by amount, not card size
  – Ability to change underlying technology while preserving API

• No Hardware Specifics in Software
  – Error Isolation, Transparent mirroring, Centralized diagnostics, etc.
  – Hardware Logging, FRU Call, Recovery: Independent of software

Data transfer between Main Memory and Storage Class Memory is via EADMF (4KB or 1MB blocks)
z/OS FLASH Use Cases

• Paging

  – z/OS paging subsystem will work with mix of internal Flash and External Disk
    • Self Tuning based on measured performance
    • Improved Paging Performance, Simplified Configuration

  – Begin Paging 1 MB Large Pages only to Flash
    • Exploit Flash’s random I/O read rate to gain CPU performance by enabling additional use of
      Large Pages. Currently large pages are not pagable.

  – Begin Speculative Page-In of 4K Pages
    • Exploit Flash’s random I/O read rate to get Improved Resilience over Disruptions.
    • Market Open, Workload Failover,
z/OS Flash Use Cases …

• Dumping

  – Minimize SVC Dump duration, System impact
    • Flash performance during SDUMP
    • Flash performance after SDUMP

  – Reduce Stand Alone Dump duration
    • Read time for paged out data
Flash for z/OS Paging Value

• Flash Express is a faster paging device compared to a hard disk

  – The value is NOT in replacing memory with flash but replacing disk with Flash

  – Flash is suitable for workloads that can tolerate paging and will not benefit workloads that cannot afford to page

  – The z/OS design for flash memory does not completely remove the virtual storage constraints created by a paging spike in the system. (Some scalability relief is expected due to faster paging I/O with flash memory.)
Typical Customer Configurations for FLASH

• Flash card pair memory size is 1.6TB
  – Min: 1 Card Pair

• Typical customer configuration is 6 to 8 LPARs per CPC and 40 GB - 80GB for paging configuration dataset size

• Even with 10 LPARs per CPC, each LPAR has 160 GB of flash memory available for its paging datasets, more than double the current typical customer configuration
  – All paging data can easily reside on Flash
  – Data will preferably go to flash and only go to disk (if any) when flash is full
  – No intelligent placement of data on internal flash needed
RSM Enhancements

• RSM Enhancements will be delivered via RSM Enablement Offering Web Deliverable (FMID JBB778H) for z/OS V1.13
  – Exploit Storage Class Memory (SCM) technology for z/OS paging and SVC dump
    • Is expected to yield substantial improvements in SVC dump data capture time
    • Remove the requirement for non-VIO local page data sets when the configuration includes enough SCM to meet peak demands
    • However, local page data sets remain required for VIO, and when needed to support peak paging demands that require more capacity than provided by the amount of configured SCM

  – Pageable 1MB Large Page Support

  – Dynamic reconfiguration support for Storage Class Memory (SCM) - target 1Q2013*

  – Optional PLPA and COMMON page data set support – target 1Q2013*

  – 2GB Large Page Support – target 1Q2013*

* All statements regarding IBM's future direction and intent are subject to change or withdrawal without notice, and represent goals and objectives only.
Flash Express PCIe Adapter Card

Must have 4 x SSD cards. Each 400 GBs
Flash Express PCIe Adapter Card with 2 ports to form a RAID 10 Mirrored Pair
Flash Express - Twin-Cable to Form a RAID 10 Mirrored Pair

- Flash Express cards are always installed in pairs
  - Maximum 4 pairs in a System

- Installed in a PCIe I/O Drawer in 2 different I/O Domains
  - Maximum of 2 pairs installed in a drawer
  - One Flash Card per Domain only
  - Greater than 2 pairs will require a second PCIe I/O Drawer
  - eConfig will reserve a slot in each Domain in case Flash Express is ordered in the future
  - Cards first installed in the front of the installed drawers (slots 1 and 14) before using the rear slots (25 and 33)

- Flash Express Cards are cabled together to form a RAID 10 Mirror for redundancy

- Data on the Flash Card is protected with a unique key stored on the Support Element (SE) harddisk
  - Only useable on the system with the key that encrypted it
  - Secure Key Store is implemented via a ‘Smart Card’ that plugs into the SE Smart Card reader
  - Smart Card contains both a unique key personalised for each system and a small Crypto engine that can perform a set of security functions within the card
  - AES encryption

Twin-Cable interconnect between the two Flash Express cards in slots 1 and 14
zEC12 Capacity and Performance Planning
The Model Capacity Identifier (MCI) is the value used by Independent Software Vendors (ISVs) to set the price for software billing. It is used to indicate the number of active CPs rather than total physical PUs delivered (purchased). The 4/5/6/7xx MCI along with the real hardware model number and the MSU value is returned when the STSI instruction is executed.

**Note:** For no CPs, the capacity setting is now 400. z196 was 700.

<table>
<thead>
<tr>
<th>HW Model</th>
<th>Model Capacity Identifier</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>H20</td>
<td>700 – 720, 6nn, 5nn, 4nn</td>
<td>Where nn = 1 to 20</td>
</tr>
<tr>
<td>H43</td>
<td>700 – 743, 6nn, 5nn, 4nn</td>
<td>Where nn = 1 to 20</td>
</tr>
<tr>
<td>H66</td>
<td>700 – 766, 6nn, 5nn, 4nn</td>
<td>Where nn = 1 to 20</td>
</tr>
<tr>
<td>H89</td>
<td>700 – 789, 6nn, 5nn, 4nn</td>
<td>Where nn = 1 to 20</td>
</tr>
<tr>
<td>HA1</td>
<td>700 – 7A1, 6nn, 5nn, 4nn</td>
<td>Where nn = 1 to 20</td>
</tr>
</tbody>
</table>
zEC12 Full and Sub-Capacity CP Offerings

- Subcapacity CPs, up to 20, may be ordered on ANY zEC12 model. If 21 or more CPs are ordered all must be full 7xx capacity.
- All CPs on a zEC12 CPC must be the same capacity.
- All specialty engines run at full capacity. The one for one entitlement to purchase one zAAP and one zIIP for each CP purchased is the same for CPs of any capacity.
- Only 20 CPs can have granular capacity but other PU cores may be characterized as full capacity specialty engines.
- For no CPs, the capacity setting is 400.
- PVU for zEC12 is 120.

MSU Sub Capacity

CP Capacity Relative to Full Capacity Uni
7xx = 100% ≈ 1514 PCI
6xx ≈ 63% ≈ 947 PCI
5xx ≈ 42% ≈ 631 PCI
4xx ≈ 16% ≈ 240 PCI
xx = 01 Through 20
zEC12 Vs z196 Capacity Comparison (Capacity Indicator 7xx)

1.25x per core, 1.5x system
System z Capacity Planning in a nutshell

Don’t use “one number” capacity comparisons!
Work with IBM technical support for capacity planning!
Customers can now use zPCR

The IBM Processor Capacity Reference (zPCR) is a free tool available for download that can be used to size your System z processors.
What's new in the LSPR for zEC12

- **Workload updates**
  - Newer levels of software - z/OS 1.13, subsystems, compilers
  - Minor tweaks to three hardware-characteristic-based workload categories
    - Based on CPU MF data from customers' z10s and z196s
- **HiperDispatch continues to be turned on for all measurements**
  - Particularly valuable on smaller z196 and zEC12 configurations due to sensitivity to L3 chip-level cache
- **LSPR - publish only the Multi-image (MI) table**
  - Median LPAR configuration for each model based on customer profile
    - Including effect of average number of ICFs and IFLs
  - MI more representative than SI for vast majority of customers
  - Basis for single-number metrics MIPs (PCIs), MSUs, SRM constants
- **Single-image (SI) table**
  - No longer published starting with z/OS 1.11 LSPR
    - Avoid confusion
  - Continues to be used in zPCR and CP3000
zEC12 Upgrades
zEC12 Upgrades

- zEC12 to higher hardware zEC12 model
  - Upgrade of zEC12 Models H20, H43, H66 and H89 to HA1 is disruptive
  - When upgrading to zEC12 HA1 all the Books are replaced
  - Conversion from Radiator-based air to Water cooled or Water to Radiator-based air cooling not available

- Any z10 EC to any zEC12
- Any z196 to any zEC12

- When a z196 with a zBX Model 002 is upgraded to zEC12, the zBX is converted to a Model 003. Additional planning required and conditions apply
zEC12 Internal I/O Infrastructure Overview
# System z I/O Interface Evolution

<table>
<thead>
<tr>
<th>Generation</th>
<th>I/O Interface</th>
</tr>
</thead>
<tbody>
<tr>
<td>z9</td>
<td>Extended Link (processor to I/O Cage)</td>
</tr>
<tr>
<td>z10</td>
<td>I/O Cage Backplane</td>
</tr>
<tr>
<td>z196</td>
<td>Coupling Link</td>
</tr>
<tr>
<td>z114</td>
<td>eSTI (IBM) → InfiniBand → PCI Express (Ind. Std.)</td>
</tr>
<tr>
<td>zEC12</td>
<td>mSTI (IBM) → InfiniBand → PCIe Gen2 (Ind. Std.)</td>
</tr>
</tbody>
</table>

- InfiniBand
- PCI Express (Ind. Std.)
- PCIe Gen2 (Ind. Std.)
System z I/O Subsystem Internal Bus Interconnect Speeds (GBps)

- **PCle**
  - zEC12/z196/z114: 8 GBps

- **InfiniBand**
  - z10/z196/z114 & zEC12 for carry forward: 6 GBps

- **STI**
  - **z9**: 2.7 GBps
  - **z990/z890**: 2 GBps
  - **z900/z800**: 1 GBps

STI: Self-Timed Interconnect

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zEC12 PCIe I/O drawer

• Introduced with z196 and z114 – July 2011
• Compact
  – Two PCIe I/O drawers occupy the same space as one I/O cage
• Increased granularity
  – Two FICON Express8S channels per feature
  – One or two OSA-Express4S ports per feature
  – One Crypto Express4S per feature
• I/O card density – 14% more capacity
  – 32 I/O card slots
• Peripheral Component Interconnect Express Generation 2 (PCIe Gen2) – 8 GBps bus
  – Infrastructure from processor book to I/O cards
• Reduced power consumption
• Designed for improved RAS
  – Symmetrical, redundant cooling across all cards and power supplies
  – Temperature monitoring of critical Application-specific integrated circuits (ASICs)
  – Concurrent add/repair of PCIe I/O drawer and adapters
ESCON Statement of Direction - February 15, 2011

• The IBM zEnterprise 196 (z196) will be the last high-end server to support ESCON channels: IBM plans not to offer ESCON channels as an orderable feature on high-end System z servers which follow the z196 (machine type 2817). In addition, ESCON channels cannot be carried forward on an upgrade to such a follow-on server.

• This plan applies to channel path identifier (CHPID) types CNC, CTC, CVC, and CBY and to feature code numbers 2323 and 2324. System z customers should continue migrating from ESCON to FICON. Alternate solutions are available for connectivity to ESCON devices.

• IBM Global Technology Services offers an ESCON to FICON Migration solution. This offering should help customers to simplify and manage a single physical and operational environment.

• Notes:
  – This Statement of Direction superseded the previous ESCON SOD in Announcement letter 110-170 of July 22, 2010. It also confirms the SOD in Announcement letter 109-230 of April 28, 2009 that “ESCON Channels will be phased out.”

  – No exceptions or RPQs. zEC12 does NOT have any code for ESCON
PRIZM is available from IBM GTS Site & Facilities as part of the EFM Service (ESCON to FICON Migration - offering # 6948-97D)

- The order process for PRIZM is the same as it is for IBM cabling systems
Where Does PRIZM Fit in the Data Center?

1. Point-to-Point FICON

2. Switched FICON

3. Cascaded and Channel Extended FICON

*PRIZM supports all ESCON control units: Tape, Printers, Com Devices, FEPs etc.*
FICON Express8S – SX and 10KM LX in the PCIe I/O drawer

- For FICON, zHPF, and FCP environments
  - CHPID types: FC and FCP
    - 2 PCHIDs/CHPIDs
- Auto-negotiates to 2, 4, or 8 Gbps
- Increased performance compared to FICON Express8
- 10KM LX - 9 micron single mode fiber
  - Unrepeated distance - 10 kilometers (6.2 miles)
  - Receiving device must also be LX
- SX - 50 or 62.5 micron multimode fiber
  - Distance variable with link data rate and fiber type
  - Receiving device must also be SX
- 2 channels of LX or SX (no mix)
- Small form factor pluggable (SFP) optics
  - Concurrent repair/replace action for each SFP

FC 0409 – 10KM LX, FC 0410 – SX

OM3

OM2

LX/LX

SX/SX

OR

IBM System z

IBM

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FICON performance on System z

I/O driver benchmark
I/Os per second
4k block size
Channel 100% utilized

I/O driver benchmark
MegaBytes per second
Full-duplex
Large sequential read/write mix
OSA-Express4S 1000BASE-T for the PCIe I/O Drawer

- OSA-Express4S 1000BASE-T Ethernet
  - Exclusive to zEC12
  - Auto-negotiation to 10, 100, 1000 Mbps
  - CHPID types
    - OSC, OSD, OSE, OSM, OSN
- Two ports
  - 1 PCHID/CHPID
- Operates at “line speed”
- Category 5 or Category 6 copper cable
- RJ-45 connector

<table>
<thead>
<tr>
<th>Mode</th>
<th>CHPID</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>OSA-ICC</td>
<td>OSC</td>
<td>TN3270E, non-SNA DFT, IPL CPCs, and LPARs, OS system console operations</td>
</tr>
<tr>
<td>QDIO</td>
<td>OSD</td>
<td>TCP/IP traffic when Layer 3, Protocol-independent when Layer 2</td>
</tr>
<tr>
<td>Non-QDIO</td>
<td>OSE</td>
<td>TCP/IP and/or SNA/APPN/HPR traffic</td>
</tr>
<tr>
<td>Unified Resource Manager</td>
<td>OSM</td>
<td>Connectivity to intranode management network (INMN) from zEC12 to Unified Resource Manager functions</td>
</tr>
<tr>
<td>OSA for NCP (LP-to-LP)</td>
<td>OSN</td>
<td>NCPs running under IBM Communication Controller for Linux (CDLC)</td>
</tr>
</tbody>
</table>
OSA-Express4S GbE and 10 GbE fiber for the PCIe I/O drawer

- 10 Gigabit Ethernet (10 GbE)
  - CHPID types: OSD, OSX
  - Single mode (LR) or multimode (SR) fiber
  - One port of LR or one port of SR
    - 1 PCHID/CHPID

- Gigabit Ethernet (GbE)
  - CHPID types: OSD (CHPID OSN not supported)
  - Single mode (LX) or multimode (SX) fiber
  - Two ports of LX or two ports of SX
    - 1 PCHID/CHPID

- Small form factor optics – LC Duplex
OSA-Express4S 10 GbE performance (laboratory)

**Inbound Streams** – 1492 Byte MTUs

- **Mixed Streams** – 1492 Byte MTUs

**Inbound Streams** – 8000 Byte MTUs

- **Mixed Streams** – 8000 Byte MTUs

Notes:
- AWM on z/OS
- z/OS is doing checksum
- 1 megabyte per second (MBps) is 1,048,576 bytes per second
- MBps represents payload throughput (does not count packet and frame headers)
Parallel Sysplex Server Coexistence

**zEC12**

Support for N-2 Only!

**z9 EC or earlier - CF & OS**
(Sysplex and STP)

Not Supported

**z9 BC or earlier - CF and OS**
(Sysplex and STP)

Not Supported

**IMPORTANT**

zEC12 can be in same STP CTN as z196, z114 and z10 servers but NOT in a STP CTN with z9 servers
zEC12 Server Time Protocol Enhancements

- Broadband Security Improvements for STP
  - Authenticates NTP servers when accessed by the HMC client through a firewall
  - Authenticates NTP clients when the HMC is acting as an NTP server
  - Provides symmetric key (NTP V3-V4) and autokey (NTP V4) authentication
    (Autokey is not supported if Network Address Translation is used)
  - This is the highest level of NTP security available
- Improved NTP Commands panel on HMC/SE
  - Shows command response details
- Telephone modem dial out to an STP time source is no longer supported
  - All STP dial functions are still supported by broadband connectivity
  - zEC12 HMC LIC no longer supports dial modems
    (Fulfills the Statement of Direction in Letter 111-167, dated October 12, 2011)
zEC12 Cryptography
• Cryptographic Coprocessor Facility – Supports “Secure key” cryptographic processing
• PCICC Feature – Supports “Secure key” cryptographic processing
• PCICA Feature – Supports “Clear key” SSL acceleration
• PCIXCC Feature – Supports “Secure key” cryptographic processing
• CP Assist for Cryptographic Function allows limited “Clear key” crypto functions from any CP/IFL
  – NOT equivalent to CCF on older machines in function or Crypto Express2 capability
• Crypto Express2 – Combines function and performance of PCICA and PCICC
• Crypto Express3 – PCIe Interface, additional processing capacity with improved RAS
• Crypto Express4S - IBM Standard PKCS #EP11
IBM has been providing Security & Encryption Solutions for over 30 years…

A History of Enterprise Security

- Hardware Cryptography: 1970
- RACF: controls access to resources and applications: 1976
- Key management built into operating system (ICSF): 1991
- Distributed Key Management System (DKMS) (1990’s)
- Intrusion Detection Services (IDS): 2001
- z/OS PKI Services: create digital certificates & act as Certificate Authority (CA) – 2002
- Multilevel Security (MLS): 2004
- Encryption Facility for z/OS: 2005
- TS1120 Encrypting Tape Drive: 2006
- LTO4 Encrypting Tape Drive: 2007
- Agreement with Certicom: 2008
- Tivoli Encryption Key Lifecycle Manager: 2009
- Self-Encrypting Disk Drives, DS8000: 2009
- System z10 CPACF Protected Key Support: 2009
- Crypto Express3 Crypto Coprocessor: 2009
- System z196 with additional CPACF encryption modes: 2010
- System zEC12 with Public Key Cryptography Standards
Overview – HW Crypto support in System zEC12

- Processor Books
- MCM
- CPACF
- PCIe I/O drawers
- Crypto Express4S
- Trusted Key Entry (TKE)
- Smart Card Readers
- Smart Cards
Crypto Express4S

- One PCIe adapter per feature
  - Initial order – two features
- FIPS 140-2 Level 4
- Installed in the PCIe I/O drawer
- Up to 16 features per server
- Prerequisite: CPACF (FC 3863)

- Three configuration options for the PCIe adapter
  - Only one configuration option can be chosen at any given time
  - Switching between configuration modes will erase all card secrets
    - Exception: Switching from CCA to accelerator or vice versa

- Accelerator
  - For SSL acceleration
  - Clear key RSA operations

- Enhanced: Secure IBM CCA coprocessor (default)
  - Optional: TKE workstation (FC 0841) for security-rich, flexible key entry or remote key management

- New: IBM Enterprise PKCS #11 (EP11) coprocessor
  - Designed for extended evaluations to meet public sector requirements
    - Both FIPS and Common Criteria certifications
  - Required: TKE workstation (FC 0841) for management of the Crypto Express4S when defined as an EP11 coprocessor
  - Supported on Crypto Express4S only
IBM Common Cryptographic Architecture (CCA) LIC Enhancement

Architected set of cryptographic functions and application programming interfaces (APIs) that provide both general-purpose functions and a broad set of functions designed specifically to secure financial transactions and keys

• Enhancements
  – Standards compliance – improved wrapping key strength
  – DUKPT for derivation of MAC and Encryption Keys
  – Secure Cipher Text Translate
  – Compliance with new Random Number Generator standards
  – EMV enhancements for applications supporting American Express cards
IBM zAware
Background

Systems are more complex and more integrated than ever

- Errors can occur anywhere in a complex system

- Difficult to detect, difficult to diagnose, symptoms / problems can manifest hours or even days later

- Problem can grow, cascade, snowball

- Volume of data is unmanageable – need information and insight.

- Systematic ‘soft failures’ (sick but not dead) much harder to detect – several allowable anomalies can build up over time
IBM zAware –
*IBM System z Advanced Workload Analysis Reporter*

- Monitors z/OS OPERLOG messages including all z/OS console message, ISV and application generated messages
- Can monitor across a sysplex
- Samples every 2 minutes.
- Reports on 10 minute time slices.
- Uses a 90 day baseline created from SYSLOG
- Detects anomalies monitoring systems miss:
  - Messages may be suppressed or rare
  - Messages may indicate a trend
- Reports on unique messages, and a “score”
- Color-coded, browser-based (IE 8, Firefox)
- XML Output consumable through published API, can drive ISV products
## IBM z/OS Solutions Address Problem Determination

<table>
<thead>
<tr>
<th>Solutions Available:</th>
<th>Rules based</th>
<th>Analytics / Statistical model</th>
<th>Examines message traffic</th>
<th>Self Learning</th>
<th>Method</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>z/OS Health Checker</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Rules based to screen for conditions</td>
</tr>
<tr>
<td>• Checks configurations</td>
<td></td>
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<td></td>
<td></td>
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<tr>
<td>• Programmatic, applies to IBM and ISV tools</td>
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<td></td>
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<tr>
<td>• Can escalate notifications</td>
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<tr>
<td><strong>z/OS PFA</strong></td>
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<td></td>
<td>Early detection</td>
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<tr>
<td>• Trending analysis of z/OS system resources, and performance</td>
<td></td>
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<td></td>
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</tr>
<tr>
<td>• Can invoke z/OS RTD</td>
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<tr>
<td><strong>z/OS RTD</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>After an incident</td>
</tr>
<tr>
<td>• Real time diagnostics of specific z/OS system issues</td>
<td></td>
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</tr>
<tr>
<td><strong>IBM zAware</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Diagnosis Useful before or after an incident</td>
</tr>
<tr>
<td>• Pattern based message analysis</td>
<td></td>
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<td></td>
<td></td>
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<tr>
<td>• Self learning</td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>• Provides aid in diagnosing complex z/OS problems, including cross sysplex, problems that may or may not bring the system down</td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
</tbody>
</table>

- IBM zAware Uniquely analyzes messages in context to determine unusual behaviors
- IBM zAware Uniquely understands and tunes its baseline to compare against your current activity
- IBM zAware does not depend on other solutions, manual coding of rules, and is always enabled to watch your system
How can IBM zAware Improve Problem Determination?

- **Identify messages indicating a possible z/OS incident is happening**
  - Which image is behaving abnormally?
    - Examines unique messages
    - High score generated by unusual messages or message patterns
  - When did this unusual behavior start?
    - For a selected 10 minute interval either the current 10 minute interval or past intervals
      - Which message ids are unusual?
      - How often did the message occur?
      - When did the message start to occur?
  - Were similar messages issued in the past?
    - Similar characteristics, Same pattern?

- **After a change has been made**
  - Are unusual messages being issued following changes?
    - New software levels (operating system, middleware, applications)
    - Updated system settings / system configurations

- **When diagnosing the cause of an intermittent problem**
  - Are new unusual messages being issued in advance of the problem?
  - Are more messages issued than expected?
  - Are messages issued out of normal pattern or context?

Find Anomalies that would be Hard to Detect

Vertical bar shows the number of unique messages in a 10 minute interval

Scoring of messages color coded from common (blue) to rare (orange)
## Snapshots – Drill Down

### System Anomaly Scores

<table>
<thead>
<tr>
<th>System</th>
<th>Anomaly Scores</th>
</tr>
</thead>
<tbody>
<tr>
<td>TICF</td>
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### Interval Contribution Score | Appearance Count | Cluster ID | Rarity Score | Time Line | Component | Message ID | Message Example |
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<thead>
<tr>
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<tr>
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<td>17</td>
<td>-</td>
<td>101</td>
<td></td>
<td>ILR</td>
<td>ILR0372</td>
<td>PAGE DATA SET HAS BEEN USED BY ANOTHER SYSTEM: 042 DATA SET NAME - SYS1.TBP00.COMMON VOLUME SERIAL - TBP00 DEVICE NUMBER - 87FC SYSTEM NAME - TICF [...] DATA SET LAST UPDATED AT</td>
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<td>-</td>
<td>101</td>
<td></td>
<td>ILR</td>
<td>ILR039A</td>
<td>PAGE DATA SET MAY BE IN USE: 032 DATA SET NAME - SYS1.TBP00.PLPA VOLUME SERIAL - TBP00 DEVICE NUMBER - 87FC SYSTEM NAME - TICF [...] DATA SET LAST UPDATED AT 083731 ON</td>
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<td>-</td>
<td>101</td>
<td></td>
<td>ILR</td>
<td>ILR031F</td>
<td>REPLY &quot;DENY&quot; TO PREVENT ACCESS, CONTINUE TO ALLOW USE OF SYS1.TBP00.PLPA.</td>
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<tr>
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<td>101</td>
<td></td>
<td>IEA</td>
<td>IEA3801</td>
<td>THIS SYSTEM IS NOW OPERATING IN STP TIMING MODE.</td>
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<td>-</td>
<td>101</td>
<td></td>
<td>AOF</td>
<td>AOF9041</td>
<td>AUTOMATION PAUSED BY OPERATOR REQUEST</td>
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<tr>
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<td>1</td>
<td>-</td>
<td>101</td>
<td></td>
<td>CNZZ</td>
<td>CNZZ033E</td>
<td>SPECIFIC MESSAGE THRESHOLD REACHED FOR IOS2511</td>
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<tr>
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<td>1</td>
<td>-</td>
<td>101</td>
<td></td>
<td>IEAVEH</td>
<td>IEAVEH074F</td>
<td>HiperDispatch is expected to be enabled but it is disabled</td>
</tr>
<tr>
<td>0.291</td>
<td>6</td>
<td>-</td>
<td>101</td>
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<td>EZZ</td>
<td>EZZ7871</td>
<td>NO MATCHING INTERFACE STATEMENTS FOR 10.103.247.18 (MP0_TICF_TW PR)</td>
</tr>
</tbody>
</table>
IBM zAware Complements an Existing Environment

- IBM zAware provides XML data to support alternative views generated by higher level managers.

- z/OSMF links to IBM zAware.

- Service Management Software
  - Tivoli

- Enterprise Management Workspace views

- Sysplex Management
  - Sysplex views
  - Management of z/OS

- IBM zAware
  - Customer controlled scope
    - Sysplex views
    - z/OS Image view
    - Closed appliance
Critical Questions Answered by IBM zAware

- When a problem occurs
  - Which z/OS image is behaving abnormally
    - Lots of unique messages
    - High score generated by unusual message ids or an unusual patterns of message ids
  - When did the z/OS image start to behave abnormally
  - For a selected 10 minute interval either the current 10 minute interval or intervals in the past
    - What message ids are unusual
    - Are messages issued in context within expected messages pattern
    - Is a component emitting unusual message ids
    - How often did the message id occur
    - Within the 10 minute interval when did the message id start t occur
  - Did the z/OS image produce the same messages for the corresponding interval in the past
    - Yesterday, last week, last month, ...

- After a change has been made
  - Are new unusual messages being issued during periods immediately following changes like
    - New software levels (operating system, middleware, applications)
    - Updated system settings / system configurations
  - Are more messages issued than expected

- When looking for the cause of a random, intermittent problem
  - Are new unusual messages being issued during periods before the problem is reported or during the periods when the problem is being reported
  - Are more messages issued then expected
  - Are messages issued out of context
All zEC12 site

- Single IBM zAware

IBM zAware can communicate with any z/OS LPAR running z/OS 1.13 with appropriate APARs installed.

Customer controlled scope
Sysplex views
z/OS Image views
Closed Appliance.
Mixed site (zEC12 and z196 or z114)

- Single IBM zAware active for site only on zEC12

IBM zAware can communicate with any z/OS LPAR running z/OS 1.13 with appropriate APARs installed

Customer controlled scope
Sysplex views
z/OS Image views
Closed Appliance
zEC12 Power and Cooling
zEC12 Overhead Power Option

Shipped separately and installed on-site to allow for door clearance

Raised Floor: Optional
Non Raised Floor: Mandatory
Co-req: Top Exit I/O option
zEC12 Cooling changes from z196

• Air Cooled Server
  – “Radiator” design replaces refrigerant cooling for cooling the processor modules
  – Cooling path has redundancy of all active components
  – Air backup for rare plumbing problem
  – Total airflow through system increased approximately 4-5%
  – Fill and Drain of coolant required for freeze protection when shipping
    • Require zEC12 Fill & Drain tool for system install

• Water cooled server
  – Now support customer water up to 20°C (was 16°C in z196)
  – From 20°C to 23°C warning messages may appear related to water temperature
  – Above 23°C will have messages and may cycle steer at some point

• All zEC12 servers have left unchanged:
  – Air flow for system is still front to back
  – Air temperature, altitude and humidity requirements are the same as z10 and z196
    (Class 1 ASHRAE). Acoustic Category 1B
zEC12 Water Cooling and Exhaust Air Heat Exchanger

• **Water Cooling Unit (WCU)**
  - Two water cooling units with independent chilled water connections
  - Designed to use using standard building chilled water, temperature range is 6-16 degrees C (43-61 degrees F).
  - Water connection utilizes quick disconnect connectors, one customer supply and return for each WCU
  - Design target is to remove 60 to 65 percent of air heat load
  - NEW Upgrades from air to water and water to air NOT supported

• **Exhaust Air Heat Exchanger**
  - Two Exhaust Air Heat Exchangers units installed on the rear of the A & Z frames
  - Designed to remove heat from the internal system water loop and from internal air exiting the server into the hot air exhaust aisle
  - Different requirements from the zBX Rear Door Heat Exchanger

• **Fill and Drain Kit**
  - Recommend one drain kit per site, FC 3378
  - Consist of FDT Pump, Benzotriazole (BTA) Reservoir Container and associated hoses

• **Quick Energy Estimator**
  - Pre-sales tool to quickly compare energy consumption between air-cooled and water-cooled options
  - Available IBM and IBM BP’s only, output can be shared with customers

IBM recommends water for the most efficient data center
zEC12 Water cooling infrastructure

Rear View – A Frame

Note: This is not the Rear Door Heat Exchanger design!
zEC12 Water Cooling Unit Details

zEC12 Water Cooling Units

Connections to the Books
(Internal system water closed-loop)
zEC12 - Introducing Radiator for Air Cooled System

• Closed loop water cooling N+1 pump system replaces modular refrigeration units (MRUs) used for air cooling in z196 and z10 EC
  – No connection to chilled water required
  – Water added to the closed loop system during installation (New Fill and Drain Tool)

• Normal operation design:
  – Heat removed by water circulating to the radiator
  – Fans exhaust heat from the radiator to room air

• Backup operation design
  – N+1 pump/blower failure: Cooling maintained by closed loop water system without “cycle steering” slow down. Concurrent repair.
  – Water cooling system failure: Cooling maintained by backup fans as in the z196 air cooled option with MRUs. “Cycle steering” slow down if needed to maintain operation. Concurrent repair
Comparing MRUs with Radiator Unit for zEC12

z196 MRU Front

zEC12 Radiator Front (NEW)

z196 MRU Rear

zEC12 Radiator Rear (NEW)
On raised floor, either radiator-based air or water cooling is supported.

There is NO overhead support for cooling water supply - return.
If zEC12 is NOT installed on a raised floor, overhead I/O, overhead power, and radiator (air) cooling options are required.

Water cooling is NOT supported. NO cables may exit at floor level.
zEC12 – Announced Operating System Support
Operating System Support for zEC12

- Currency is key to operating system support and exploitation of future servers
- The following releases of operating systems are supported on zEC12
  (refer to PSP buckets for any required maintenance):

<table>
<thead>
<tr>
<th>Operating System</th>
<th>Supported levels</th>
</tr>
</thead>
<tbody>
<tr>
<td>z/OS</td>
<td>• z/OS V1R13 with PTFs (Exploitation)</td>
</tr>
<tr>
<td></td>
<td>• z/OS V1R12 with PTFs (Exploitation)</td>
</tr>
<tr>
<td></td>
<td>• z/OS V1R11 with PTFS (Toleration, Lifecycle extension required after 09/12)</td>
</tr>
<tr>
<td></td>
<td>• z/OS V1R10 (Toleration, Lifecycle Extension Required)</td>
</tr>
<tr>
<td>Linux on System z</td>
<td>• Planned with the following distributions:</td>
</tr>
<tr>
<td></td>
<td>• SUSE SLES 10 and SLES 11</td>
</tr>
<tr>
<td></td>
<td>• Red Hat RHEL 5 and RHEL 6</td>
</tr>
<tr>
<td>z/VM</td>
<td>• z/VM 5.4, 6.1, and 6.2 will support zEC12 with PTFs</td>
</tr>
<tr>
<td>z/VSE</td>
<td>• z/VSE compatibility with PTFs, support for:</td>
</tr>
<tr>
<td></td>
<td>• z/VSE 4.3</td>
</tr>
<tr>
<td></td>
<td>• z/VSE 5.1</td>
</tr>
<tr>
<td>z/TPF</td>
<td>• V1.1</td>
</tr>
</tbody>
</table>

- Support for p Blades in zBX Model 003
  - AIX 5.3 Technology Level 12 or higher, AIX 6.1 Technology Level 5 or higher, AIX 7.. All with PowerVM™ Enterprise Edition
- Support for Linux and Windows* environments on select System x blades in zBX Model 003
  - 64 bit version support only
  - Red Hat RHEL 5.5 and higher, 6.0 and higher and SLES 10 (SP4), 11 SP1 and higher
  - Microsoft Windows Server 2008 R2 and Microsoft Windows Server 2008 (SP2) (Datacenter Edition recommended)
Statements of Direction

All statements regarding IBM's plans, directions, and intent are subject to change or withdrawal without notice. Any reliance on these Statements of General Direction is at the relying party’s sole risk and will not create liability or obligation for IBM.
Statements of Direction (SODs)

- **The IBM zEnterprise EC12 will be the last high-end server to support connections to an STP Mixed CTN.** This includes the Sysplex Timer(R) (9037). After zEC12, servers that require time synchronization, such as to support a base or Parallel Sysplex(R), will require Server Time Protocol (STP), and all servers in that network must be configured in STP-only mode.

- **Removal of support for Ethernet half-duplex operation and 10 Mbps link data rate:** The OSA-Express4S 1000BASE-T Ethernet feature is planned to be the last copper Ethernet feature to support half-duplex operation and a 10 Mbps link data rate. The IBM zEnterprise EC12 servers are planned to be the last IBM System z servers to support half-duplex operation and a 10 Mbps link data rate for copper Ethernet environments. Any future 1000BASE-T Ethernet feature will support full-duplex operation and auto-negotiation to 100 or 1000 Mbps exclusively.

- **Removal of ISC-3 support on System z:** The IBM zEnterprise EC12 is planned to be the last high-end System z server to offer support of the InterSystem Channel-3 (ISC-3) for Parallel Sysplex environments at extended distances. ISC-3 will not be supported on future high-end System z servers as carry forward on an upgrade. Previously we announced that the IBM zEnterprise 196 (z196) and IBM zEnterprise 114 (z114) servers were the last to offer ordering of ISC-3. Enterprises should continue migrating from ISC-3 features (FC 0217, FC 0218, FC 0219) to 12x InfiniBand (FC 0171 - HCA3-O fanout) or 1x InfiniBand (FC 0170 - HCA3-O LR fanout) coupling links.

- **Removal of OSA-Express3 support on System z:** The IBM zEnterprise EC12 is planned to be the last high-end System z server to offer support of the Open System Adapter-Express3 (OSA-Express3 #3362, #3363, #3367, #3370, #3371) family of features. OSA-Express3 will not be supported on future high-end System z servers as carry forward on an upgrade. Enterprises should continue migrating from the OSA-Express3 features to the OSA-Express4S features (FC 0404, FC 0405, FC 0406, FC 0407, FC 0408).

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Statements of Direction (SODs)

- **Removal of Crypto Express3 support on System z**: The IBM zEnterprise EC12 is planned to be the last high-end System z server to offer support of the Crypto Express3 feature (FC 0864). Crypto Express3 will not be supported on future high-end System z servers as carry forward on an upgrade. Enterprises should begin migrating from the Crypto Express3 feature to the Crypto Express4S feature (FC 0865).

- **IBM Java exploitation of IBM zEnterprise EC12 (zEC12) functions**: IBM plans for future maintenance roll-ups of IBM 31-bit and 64-bit SDK7 for z/OS Java(TM) Technology Edition, Version 7 (5655-W43 and 5655-W44) (IBM SDK7 for z/OS Java), to provide exploitation of new IBM zEnterprise EC12 features, including: Flash Express and pageable large pages, Transactional Execution Facility, Miscellaneous-Instruction-Extension Facility, and 2 GB pages. In addition, IBM SDK7 for z/OS Java is available for use by IBM middleware products running Java, such as IBM IMS 12 (5635-A03), IBM DB2 10 for z/OS (5605-DB2), and the Liberty profile of IBM WebSphere Application Server for z/OS v8.5 (5655-W65); and is planned for use by a future release of CICS Transaction Server for z/OS.

- **IBM System z Integrated Information Processor (zIIP) and IBM System z Application Assist Processor (zAAP) Simplification**: IBM zEnterprise EC12 is planned to be the last high-end System z server to offer support for zAAP specialty engine processors. IBM intends to continue support for running zAAP workloads on zIIP processors ("zAAP on zIIP"). This is intended to help simplify capacity planning and performance management, while still supporting all the currently eligible workloads. In addition, IBM plans to provide a PTF for APAR OA38829 on z/OS V1.12 and V1.13 in September 2012 to remove the restriction that prevents zAAP-eligible workloads from running on zIIP processors when a zAAP is installed on the server. This is intended only to help facilitate migration and testing of zAAP workloads on zIIP processors.
Statements of Direction (SODs)

- **IBM plans to provide new capability within the Tivoli Integrated Service Management family of products** designed to leverage analytics information from IBM zAware, and to provide alert and event notification.

- **CPU Management for System x blades**: IBM intends to deliver workload-aware optimization for IBM System x Blades in the zBX. This allows virtual CPU capacity to be adjusted automatically across virtual servers within a hypervisor, helping to insure that System x resources in the zBX are executing to the defined SLAs.

- **Automated Multi-site Recovery**: IBM intends to deliver automated multi-site recovery for zBX hardware components based upon GDPS technologies. These capabilities will help facilitate the management of planned and unplanned outages across IBM zEnterprise EC12.

- **IBM Systems Director Standard Edition for Linux on System z**: IBM intends to deliver new functionality in IBM Systems Director Standard Edition for Linux on System z to support IBM’s zBX. Such planned new capabilities will be designed to provide virtual image management and enhanced energy management functions for the Power Systems and System x blades.

- **DB2 continues to deliver extremely high availability, security, and resiliency with its deep integration with z/OS on System z servers**: Beyond the existing DB2 support for zEC12 DB2 plans further enhancements designed to improve performance in two ways: 1) using pageable large (1 MB) pages and Flash Express and 2) enabling support of 2 GB pages.

- **IBM intends to update CICS Transaction Server for z/OS**, providing new application, platform and policy capabilities that can help clients build private clouds from new and existing CICS applications. This capability is intended to assist CICS clients deploy new and updated CICS applications faster, more easily, and with greater levels of confidence. For more information, please refer to Software Announcement dated August 21, 2012.

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IBM zEnterprise EC12 in an information-centric world

**Operational analytics to enable business opportunities**
- Most sophisticated data warehousing and analytics solutions with the fastest query performance in the market
- Leverage your data to build competitive advantage

**Trusted resilience for unmatched security and reliability**
- Most secure system with 99.999% reliability
- Unified platform for rapid development of secure applications end-to-end

**Efficiency at scale**
- Most efficient and fastest system for mission-critical workloads
- Increased efficiency will free up IT resources to focus on new services to drive growth
- Hybrid architecture enables rapid cloud deployment
THANK YOU