zSeries 900
S/390 Multiprise 3000 Enterprise Server
S/390 Coupling Facilities C01/C02/C03/C04/C05
S/390 Multiprise 2000
S/390 Application StarterPak
S/390 Parallel Enterprise Servers Rn1/Rn2/Rn3
S/390 Parallel Transaction Server - E0n and P0n

Purpose and Description For DR36J/Version 1.7.0
December 6, 2000

With CPC System Code: EC H25128
and HMC System Code: EC H25126

With CPC EC H25117 + MCLs
and HMC EC H25122 + MCLs
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1.0 Purpose and Description for DR36J/Version 1.7.0 (CPC System Code EC H25128 with HMC System Code H25126)

1.1.1 Overview of Customer and/or Service Enhancements

DR36J/Version 1.7.0 (CPC system code EC H25128 with HMC system code EC H25126) includes the following customer and/or service enhancements for the subject systems:

- Engineering change (EC) considerations for:
  - CPC EC H25117 + MCLs
  - HMC EC H25122 + MCLs
- For the zSeries 900
- For earlier 9672/9674/2003/3000/7060 Models
- HSA considerations
- Miscellaneous lower level ECs included in
- Input/output configuration program (IOCP) considerations
- Preventive service planning (PSP) bucket considerations

Important

This statement of enhancements assumes that the customer has all the necessary hardware and software prerequisites and corequisites. EC support for features does not include the feature itself.

1.1.2 Engineering Change (EC) Considerations

CPC system code EC H25128 with HMC system code EC H25126 for zSeries 900 includes the following Central Processor Complex (CPC) and Hardware Management Console (HMC) Licensed Internal Code (LIC) engineering change (EC) and Microcode Load (MCL) levels:

- CPC level: EC H25117 + MCLs
- HMC level: EC H25122 + MCLs

HMC system code EC H25126 for the S/390 Multiprise 3000 Enterprise Server, Parallel Enterprise Server - Generations 3, 4, 5, and 6, Coupling Facility Models C01 - C05, Multiprise 2000, Application StarterPak, Parallel Enterprise Server - RN1, RN2, RN3 Models, and Parallel Transaction Server models includes the following Hardware Management Console (HMC) Licensed Internal Code (LIC) engineering change (EC) and Microcode Load (MCL) levels:

- HMC level: EC H25122 + MCLs

To verify that the enhancements described in this document apply to your system, display the LIC EC levels running on the CPC and the HMC.

1.1.2.1 CPC EC H25117 + MCLs

You can display the LIC EC and MCL level of the system’s CPC as follows:

1. Select the CPC
2. Drag and drop the CPC onto the System Information object in the Change Management Tasks list.
A list of CPC EC levels and (activated) MCL levels displays. Verify that EC level H25117 is in this list.

1.1.2.2 HMC EC H25122 + MCLs
You can display the LIC EC and MCL level of the system’s HMC as follows:
1. Open (double-click on) the Console Actions object
2. Open (double-click on) the View Console Information object
   A list of HMC EC levels and (activated) MCL levels displays. Verify that EC level H25122 is in this list.

1.1.3 For the zSeries 900
IBM® is introducing the IBM zSeries 900. The IBM zSeries 900 provides new tools for managing e-business, new application flexibility, and new technology.

The zSeries 900 offers numerous upgrade options from S/390 9672 G5 and G6 models. S/390 operations are fully compatible with the new architecture - z/Architecture, based upon 64-bit real addressing. S/390 applications are fully compatible with z/Architecture.

Attention
Some support described in this Purpose and Description will be delivered with LIC patches. You should plan on these patches being disruptive. Content and planned availability are as follows:
- LIC patch planned availability 01/31/01 will provide support for:
  - Upgrading a 9672 G5/G6 to a z900 server.
  - Concurrent feature adds to a z900 server.
  - Ordering a z900 with CBU / CUoD.
- LIC patch planned availability 03/31/01 will provide support for:
  - Model 100
  - Native FICON (FC CHPID type)
  - Peer mode coupling (ISC-3 and ICB-3), see note #1
  - 512K HSA subchannels and 63K per image subchannels, see note #2
  - Intelligent Resource Director (IRD)
  - Workload License Charges
  - Extended Translation Facility (UNICODE)
  - FICON Shortwave feature

Notes:
1. Prior to installing the LIC patch, the user should not configure peer coupling channels (CFP and CBP).
2. Prior to installing the LIC patch, the user should closely monitor the device reports from HCD or IOPC to ensure planned configurations do not exceed 288K HSA or 36K image subchannels. Also, when activating dynamic I/O on the z900, the user should ensure that the dynamic expansion percentage when applied to the defined configuration will not exceed 288K HSA or 36K image subchannels. Neither HCD, IOPC, or the machine will prevent Power-On-Reset with greater than the supported number of subchannels.
1.1.3.1 The Benefits

Price-To-Performance Ratio

The zSeries 900, supported by WorkLoad Manager and logical server enhancements, provides self-managing flexibility and can reduce the cost of computing.

The zSeries 900 I/O subsystem has been designed to support an I/O bus bandwidth from 8 to 24 GB/second. This bandwidth supports connection to high speed storage and communications networking devices. The zSeries 900 coupling links support bandwidth requirements up to 1000 MB/second for shorter distance Integrated Cluster Bus (ICB) links, and, up to 200 Mbytes/second for InterSystem Coupling (ISC) links.

The zSeries 900 provides the following:

- The coupling facility model with increased capacity, newer links, and upgrade capability.
- New Coupling Links: New Integrated Cluster Bus-3 (ICB-3) links, New InterSystem Coupling-3 (ISC-3) links, and New Internal Coupling-3 (IC-3) links. ISC-3, ICB-3, and IC-3 links support a new enhanced performance mode called "Peer Mode". ISC-3 links may also be configured (using CHPID type in the IOCDS) for Compatibility Mode. In addition, ICB-2 links may be ordered for Compatibility Mode ICB connections.
- Intelligent Resource Director which includes LPAR CPU Management, Dynamic Channel Path Management and Channel Subsystem Priority Queuing
- Managed System Infrastructure for installing and configuring z/OS and products running on z/OS.
- Extended Remote Copy support for the Geographically Dispersed Parallel Sysplex

The z/Architecture

A new z/Architecture, based upon 64-bit real addressing, has been crafted for the zSeries 900.

WorkLoad Manager clustering introduces control of clusters of logical partitions, allocating processors, memory, channel paths, and channel and controller work priority.

A new 20 Processor Unit (PU) Multichip Module (MCM) and new 12 Processor Unit (PU) Multichip Module (MCM) are the cornerstones for the zSeries 900, from a 1-way processor up to a 16-way model.

IBM’s 64-bit z/Architecture:

- Enables optimal use of memory resources
- Provides for migration flexibility
- Uses a single level of OS/390 operating system across an entire enterprise
• Allows non-disruptive test and migration and provides for ease of transition for systems support staff
• Ensures maximum transparency to the operating system and complete transparency to system applications.

The z/Architecture allows the zSeries 900 to operate as:
• As a Multi-System Server
• As a Discrete Server
• As a Cluster of Independent Servers
• As Virtual Images

Enhanced CPC Packaging to Better Address Business Processing Needs

The zSeries 900 general purpose models are:
• Machine type: 2064
  – Models:
    - zSeries 900 20 PU models: models 1C1-1C9 and 110-116
    - zSeries 900 12 PU models: models 101-109
  
  Note: special bid models 1C1-1C9 are capacity backup models. A Special Bid Contract is required and the model must be appropriately configured.

The zSeries 900 coupling facility model (available 1Q01) is:
• Machine type: 2064
  – Model: 100
    - 1-9 way coupling facilities

You can upgrade current 9672 R06 models to the zSeries 900 coupling facility model. In addition, upgrades from the coupling facility model to the general purpose models are available.

1.1.3.2 Design Highlights

zSeries 900 General Purpose Models

The design of these models supports:
• z/Architecture™
• ESA/390™ architecture (ESA/390 or ESA/390 TPF)
• Parallel Sysplex
• Intelligent Resource Director (IRD)
• Hardware Management Console control
• Logically partitioned (LPAR) operating mode
• Internal Coupling Facility CPs (ICFs)
• Workload based pricing
• LINUX
• ESCON Architecture and technology for the ESCON channels
• FICON Architecture and FICON channels
• Parallel channels
• Coupling links
  – InterSystem Coupling-3 (ISC-3) links
  – Integrated Cluster Bus (ICB-3 and ICB-2) links
  – Internal Coupling-3 (IC-3) links
• IEEE Floating Point operations
• Increased number of subchannels (over 9672 G5 and G6)
• Multiple Image Facility (MIF)
• Cryptographic coprocessor features
• Open Systems Adapter-2 (OSA-2) features
• Open Systems Adapter-Express (OSA-Express) features
• Data compression
• Dynamic I/O configuration
• CHPID assignment
• Dynamic CHPID management
• Internal Battery Feature
• Power Sequence Control
• Sysplex Timer® attachment
• Subspace Group facility
• Dedicated Move Page Engine
• Fast Sync/Data Mover
• Immediate and Relative Instruction facility
• Perform Locked Operation facility
• Logical string assist
• Modified Operating Environments
• Capacity upgrade on demand (CUoD)
• High levels of reliability, availability, and serviceability
• Online information
• Information in IBM Resource Link™

Note: The zSeries 900 does not support
• Asynchronous Data Move Facility (ADMF)
• Integrated Coupling Facility Migration (ICMF)

zSeries 900 Coupling Facility Model

The design of these models supports:
• Logically partitioned (LPAR) operating mode that allows you to define coupling facility logical partitions. You can define up to 15 logical partitions.
• CHPID assignment
• Internal Coupling Facility CPs (ICFs)
• Coupling links
  – InterSystem Coupling-3 (ISC-3) links
  – Integrated Cluster Bus (ICB-3 and ICB-2) links
• Parallel Sysplex Coupling Facility Control Code (CFCC)
• High levels of reliability, availability, and serviceability
• Online information
1.1.3.3 Some Design Details

Modes of Operation

zSeries 900 general purpose models CPCs provide the z/Architecture and ESA/390 (and ESA/390 TPF) architectures in two modes of operation:

- Basic mode
- LPAR mode

With z/Architecture or ESA/390 architecture (which includes the functions of ESA/370 architecture), these models have problem-program compatibility with S/360, S/370, and 4300 processors. They can access virtual storage in multiple address spaces and data spaces. This extends addressability for system, subsystem, and application functions that use z/Architecture or ESA/390 architectures.

Intelligent Resource Director (IRD)

Intelligent Resource Director (IRD) is a function which optimizes your workload's resource utilization across multiple logical partitions.

IRD provides the ability to dynamically manage workloads within multiple logical operating system images executing on a single zSeries 900, as a single large-scale compute resource, with dynamic workload management and physical resource balancing built into the native operating system and underlying hardware.

With IRD, z/OS WLM and WLM will exploit Parallel Sysplex technologies to monitor performance of workloads on multiple images against those workload goals. z/OS WLM will then interact with the PR/SM hypervisor, directing PR/SM to dynamically adjust the physical CPU and I/O resource allocation of the hardware across the multiple operating system instances, without requiring Parallel Sysplex data-sharing to achieve these benefits, and totally transparent to your workload applications.

IRD not only combines PR/SM, z/OS WLM, and Parallel Sysplex for LPAR CPU management, but it also includes two additional zSeries 900 exclusives: Dynamic Channel Path Management (DCM), and (Channel) I/O Subsystem Priority Queuing to increase business productivity.

Hardware Management Console

The Hardware Management Console is a PC/ISA bus PC (Pentium Processor) running OS/2, Communications Server for OS/2, a remote control systems management product, and the Hardware Management Console Application (HMCA).

The Hardware Management Console hardware configuration includes the following hardware requirement minimums:
Some earlier CMOS models may have the 6862 K1U model without the DVD RAM. If these systems are updated to zSeries 900 models, it will require an MES to exchange the CD and the ROC drives for the DVD RAM. PC models older than that require replacement of the Hardware Management Console when a zSeries 900 is to be installed.

**LINUX Support**

You can run LINUX natively in either basic mode or in a logical partition, or as a guest under VM/ESA. A fourth way to execute LINUX on zSeries 900 models is with the S/390 Virtual Image Facility for LINUX. You can isolate your LINUX on a zSeries 900 in its own workspace, using the IBM S/390 Integrated Facility for LINUX - a hardware option for capacity dedicated to LINUX workload. The S/390 Virtual Image Facility for LINUX also works in conjunction with the hardware facility for LINUX.

The IBM S/390 Integrated Facility for LINUX together with the S/390 Virtual Image Facility for LINUX, enable you to:

- Add processing capacity dedicated to running LINUX on most models of the zSeries 900
- Run multiple LINUX images independently of the traditional z/Architecture or ESA/390 workload, with associated savings of IBM z/Architecture and S/390 software charges
- Define many virtual LINUX images on fewer real zSeries 900 resources

**Connectivity Enhancements**

The zSeries 900 provides new Inter-System Coupling (ISC-3), Integrated Cluster Bus (ICB-3), and Internal Coupling (IC-3) Link Designs

Two modes of ISC-3 operation (defined using HCD/IOCP) and 2 ICB features are now available: Peer Mode and Compatibility Mode.

- **Peer Mode** supports coupling between zSeries 900s and provides both sender and receiver capability on the same link. Peer links provide up to 7 expanded buffer sets (compared to 2 buffers with G5 and G6 servers). With these design

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**Table 1-1. New Build Hardware Management Console Hardware Minimum Requirements**

<table>
<thead>
<tr>
<th>Hardware</th>
<th>Requirement</th>
</tr>
</thead>
<tbody>
<tr>
<td>General</td>
<td>Optional display monitor</td>
</tr>
<tr>
<td></td>
<td>Keyboard</td>
</tr>
<tr>
<td></td>
<td>Mouse</td>
</tr>
<tr>
<td></td>
<td>Parallel printer port</td>
</tr>
<tr>
<td>PC</td>
<td>6862 K1U</td>
</tr>
<tr>
<td>Processor</td>
<td>400 MHZ Pentium P2</td>
</tr>
<tr>
<td>Harddisk</td>
<td>4.5 GB</td>
</tr>
<tr>
<td>Memory</td>
<td>128 MB ECC</td>
</tr>
<tr>
<td>Media</td>
<td>4.7 Gb DVD RAM</td>
</tr>
</tbody>
</table>
improvements, the new Peer Mode ISC-3 connections perform at 200 MB/second for distances less than 10 km (compared to former ISC capability of 100 MB/sec) and the new Peer Mode ICB-3 connections perform at 1000 MB/second (compared to former ICB capability of up to 333 MB/sec). When coupling within a zSeries 900, the Internal Coupling-3 channel (IC-3 links which perform at a rate of 1250 MB/second) can be shared among several LPARs and one ICF. In peer mode, the zSeries 900 models support a maximum of up to 32 ISC-3 links. In peer mode, up to 16 ICB-3 links may be ordered on the zSeries 900 models.

- **Compatibility Mode** supports coupling between zSeries 900s and S/390 Parallel Sysplex Servers. ISC-3 links defined in Compatibility Mode perform at 100 MB/second. ICB-2 links which can only operate in Compatibility Mode perform at 333 Mbytes/second. In compatibility mode, the zSeries 900 models support a maximum of 32 ISC-3 links. In compatibility mode, up to 8 ICB-2 links may be ordered on general purpose models; up to 16 ICB-2 features may be ordered on the coupling facility model.

**Notes:**

1. While compatibility mode can be used between zSeries 900s, IBM recommends, whenever possible, using peer mode when coupling between zSeries 900s.
2. There is a combined system maximum of 32 coupling links composed of ISC-3, ICB-3, and ICB-2 links.

ISC-3 links allow coupling over a distance of 10 km.

**OSA Enhancements**

The OSA function provides for direct LAN attachment to the CPC. OSA enhancements on the zSeries 900 include:

- **TCP/IP Addressing**
  
  For the OSA-Express features, the maximum number of IP addresses has been increased to 512 IP addresses per port, from the previous 9672 G5 and G6 maximum of 16 IP addresses per port.

- **ARP Function**
  
  Address Resolution Protocol (ARP) is a new Internet Protocol (IP) used to dynamically map IP addresses to physical hardware Media Access Control (MAC) on addresses.

- **Extension to the SNMP Support**
  
  A Management Information Base (MIB) extension is now being offered for OSA-Express Gigabit Ethernet and Fast Ethernet QDIO connections, and for OSA-Express 155 ATM whether the connection is QDIO (Ethernet LAN Emulation only) or non-QDIO.

  Now the raw SNMP information can be passed from the OSA-Express features to Communications Server, which can then build the appropriate SNMP information.
• SNA/APPN/HPR Enhanced Connectivity

For the OSA-Express features, the number of supported PUs has been increased to 4096 PUs per physical port, for a total of 8192 PUs per feature on the zSeries 900.

Capacity Upgrade on Demand Enhancements

Capacity Upgrade on Demand (CUoD), available on most general purpose models, provides the ability to add one or more Central Processors (CP’s) and virtual servers dynamically and non-disruptively. Improving on IBM's 9672 G6 server's Capacity Upgrade on Demand capability, CUoD now provides more flexible growth of I/O connectivity. Installations may non-disruptively install FICON and ESCON channels, OSA-Express ATM 155, Gb Ethernet, and Fast Ethernet connections, Dual PCI Cryptographic Coprocessors, and InterSystem Coupling-3 links and Integrated Cluster Bus (2 and 3) links. You should use Plan-Ahead to insure you have enough I/O slots for future needs.

1.1.3.4 Availability

The standard features that provide a high level of availability include:

• Brand Upgrade Preparation: (Using I/O Configuration Definitions to prepare a 9672 G5 or G6 for upgrade to a zSeries 900)
• Enhanced Processor Design
• Larger Logic Modules
• Capacity Upgrades on Demand
• Fault Tolerant Design
• Auto-Switchover for Support Element
• 2nd and 3rd SAP Standard
• Processor Unit (PU) Sparing
• Application Preservation
• CMOS Cryptographic Coprocessor Enhancements
• Dynamic ICF Expansion
• Dynamic Coupling Facility Dispatching
• Error Correction Code (ECC)
• Enhanced Dynamic Memory Sparing
• LPAR Dynamic Storage Reconfiguration (DSR)
• Enhanced LPAR Dynamic Storage Reconfiguration
• Subsystem Storage Protect
• Enhanced Storage Protect Keys
• Memory Scrubbing
• Partial Memory Restart
• Dynamic I/O Configuration
• ESCON Port Sparing
• Concurrent Maintenance/Upgrade for Coupling
• Concurrent Channel Upgrade
• Partial I/O Restart
• Dual Power Feeds
• Redundant Power and Thermal Subsystems
• Redundant Cage Controllers
• Enhanced Cache Recovery
• External Time Reference
• Concurrent Hardware Maintenance
• Concurrent Licensed Internal Code (LIC) Patch Enhancements
• Electronic Service Agent (Service Director)

The optional features that provide a high level of availability include:

• Internal Battery Feature (IBF)
• Redundant Coupling Links
• Capacity BackUp (CBU)

1.1.3.5 Hardware Description

zSeries 900 Models Frame Configuration

The zSeries 900 frames are enclosures built to Electronic Industry Association (EIA) standards. The “A” and “Z” frames contain two cage positions. In the “A” frame, the top cage position contains a single Central Processor Complex (CPC) and its associated processing units (CPs, ICFs, IFLs), system assist processor(s) (SAPs), storage, and power components. The bottom cage position may only contain an I/O expansion cage for channel attachment capability. In the “Z” frame, both the top and bottom cage positions may only contain I/O expansion cages. The “Z” frame can contain up to two I/O expansion cages. Frame “B” contains the optional Integrated Battery Features (up to 6). Frame “B” is attached to frame “A”, and is only available as a factory installed option.

The zSeries 900 general purpose models are only available as a single CPC in a one, two, or three frame configuration depending on the I/O configuration and the inclusion of an optional Integrated Battery Feature (IBF). The minimum configuration of the zSeries 900 general purpose models consists of a single frame, the “A” frame, containing two cages, the CPC cage and one I/O expansion cage.

The zSeries 900 coupling facility model is only available as a single CPC in a one or two frame configuration depending on the inclusion of an optional Integrated Battery Feature (IBF). The “A” frame bottom cage position may contain an I/O expansion cage required for channel attachment capability. The minimum configuration of the zSeries 900 coupling facility model consists of a single frame, the “A” frame, which contains a single cage, the CPC cage.

Central Processor Complex (CPC) Cage

The base Central Processor Complex (CPC) board consists of specialized modules and cards, that provide processing unit (CPs, ICFs, IFLs), storage, channel, voltage and power control resources, Sysplex Timer attachment capability, and ICB connections.

Components which plug into the CPC board include:

• System Multi Chip Modules
• Memory cards
• CMOS Cryptographic Coprocessor chips
• Distributed Converter Assembly cards
• OSC/ETR cards
• CAP/STI card
• STI-G card
• STI-H card
I/O Subsystem

An improved I/O subsystem has been implemented on the zSeries 900 that increases the throughput of the system and also significantly reduces configuration management complexity and cost. The highlights of these improvements are:

- I/O throughput improved 3X over G5/G6
- Denser packaging that increases the number of FICON channels by 3X over G5/G6

zSeries 900 general purpose models can support a mix of ESCON, FICON, parallel, OSA-2, OSA-Express, Integrated Cluster Bus (ICB-3 and ICB-2), Internal Coupling-3 (IC-3), and InterSystem Coupling-3 (ISC-3) channels. The zSeries 900 coupling facility model supports InterSystem Coupling-3 (ISC-3) channels and Integrated Cluster Bus (ICB-3 and ICB-2) channels.

I/O expansion cage FC 2023

The FC 2023 I/O cage is designed specifically to support the new I/O feature codes introduced for the zSeries 900.

The FC 2023 I/O expansion cage contains the following cards:

- The Distributed Converter Assembly card
- The STI-M card
- ISC-3 Mother cards
- ISC-3 Daughter cards
- ESCON FC 2323 channel cards

**Note:** The 16-port ESCON Feature Code is 2323. Ports are ordered in increments of 4, with the ports activated via LICCC. The port ordering feature is 2324.

- FICON channel cards
- Dual PCI CC cards
- OSA-Express channel cards
  - Gigabit Ethernet cards
  - ATM cards
  - Fast Ethernet cards
- Power Sequence Control card

**Note:** On an upgrade, all OSA-Express cards currently plugged in a 9672 G5 or G6 server will be replaced by new OSA-Express cards which are pluggable in the FC 2023 I/O expansion cage. This is also true for FICON, Dual PCI CC, and Hiperlinks/Coupling links. On an upgrade, the 4-port ESCON may or may not be replaced with a 16-port ESCON, depending on the number of ports ordered.

I/O expansion cage FC 2022

The FC 2022 I/O cage uses some of the same cage hardware as the FC 2020 and FC 2021 I/O cages used in the 9672 G5/G6 products. To make the older I/O cage compatible with the new power subsystem communications, there are two new DCA cards and the UPC card is replaced by an extender card. The DCAs now communicate directly with the service network, a function performed by the UPC in previous products.
The FC 2022 I/O expansion cage contains the following cards:

- Distributed Converter Assembly card
- Fast Internal Bus Buffer
- Channel driver cards
- ESCON FC 2313 cards
- Parallel channel cards
- OSA-2 cards:
  - FDDI cards
  - Token Ring cards

Notes:

1. Conversion from a 9672 I/O cage is not available as a field upgrade. If you require legacy I/O or are transferring I/O features to the new system, a new FC 2022 I/O cage is shipped.

2. Existing I/O cards will be retained only if they fall within the zSeries 900 allowable features list, and plugged into the new FC 2022 I/O expansion cage. All other cards will be converted to the zSeries 900 designed features and will be plugged in the FC 2023 I/O expansion cage.

The Support Element Console

A second SE, the Alternate SE, is standard on the zSeries 900 models. The Alternate SE is configured the same as and serves as a back-up to the primary SE.

The SEs communicate with the CPC and with each other through the service network.

1.1.3.6 Hardware Configuration for the General Purpose Models

This section describes the hardware configurations for the general purpose models.

zSeries 900 general purpose models provide the following hardware elements:

- One Central Processor Complex (CPC)
- Integrated CPs
  - 1 to 9 CPs on 20 PU models 1C1-1C9 (requires a Special Bid contract)
  - 10 to 16 CPs on 20 PU models 110-116
  - 1 to 9 CPs on 12 PU models 101-109

Note: Models 1C1 - 1C9 contain reserved PUs for capacity back up CPs.

- Cryptographic Coprocessors
  - CMOS cryptographic coprocessors
    - 2 integrated CMOS crypto chips
  - Optional Dual PCI cryptographic coprocessors
    - 0 minimum; 16 maximum; available in increments of 2

- Integrated SAPs
  - 3 SAPs assigned in 20 PU models
  - 2 SAPs assigned in 12 PU models

Note: More SAPs can be purchased and defined on some models.

- Memory:
- Models 101-109
  - 5GB minimum; 32GB maximum
  Valid memory configurations are 5GB, 6GB, 7GB, 8GB, 10GB, 12GB, 14GB, 16GB, 20GB, 24GB, 28GB, and 32GB
- Models 1C1-1C9 and 110-116
  - 10GB minimum; 64GB maximum
  Valid memory configurations are 10GB, 12GB, 14GB, 16GB, 20GB, 24GB, 28GB, 32GB, 40GB, 48GB, 56GB, and 64GB
- Up to 15 logical partitions (LPs) are supported
  - Up to 32 Internal Coupling channel definitions are supported
- One Hardware Management Console (up to three additional optional Hardware Management Consoles are available) and two Internal Support Elements
- A Token-Ring Network Multistation Access Unit (MAU) or Ethernet hub
- A Modular Cooling Unit (MCU)
- Optional Internal Battery Feature (IBF)
  - 0 minimum; up to 3 pairs optional
- Optional orderable SAPs on some models
- Optional orderable ICFs on some models
- Optional orderable IFLs on some models
- Optional Power Sequence Control
- Sysplex Timer attachment
- Channels:
  
  **Note:** ISC-3 and 16-port ESCON are purchased via port ordering. Parallel, FICON, OSA-2, OSA-Express, ICB-3, and ICB-2 are purchased at the feature code level. ESCON FC 2313 is carried forward from a G5/G6 upgrade.
  - Parallel channels:
    - 0 minimum; 96 maximum; available in increments of 4
    Parallel channel attachment is through 78 pin D-shell connectors.
  - ESCON FC 2323 channels:
    - 0 minimum; 256 maximum; available in port increments of 4.
  - ESCON FC 2313 channels:
    - 0 minimum; 256 maximum; carried forward from G5/G6 upgrades in increments of 4.
  - FICON channels:
    - 0 minimum; 96 maximum; available in increments of 2.
  - OSA-2 channels:
    - 0 minimum; 12 maximum; available in increments of 1.
  - OSA-Express channels:
    - 0 minimum; 24 maximum; available in increments of 2.
- InterSystem Coupling-3 (ISC-3) channels:
  - 0 minimum; 32 maximum; available in increments of 1
- Integrated Cluster Bus-3 (ICB-3) channels:
  - 0 minimum; 16 maximum; available in increments of 1
- Integrated Cluster Bus-2 (ICB-2) channels:
  - 0 minimum; 8 maximum; available in increments of 1
- The Channel Subsystem (CSS) for general purpose models may consist of numerous combinations of ESCON, parallel, FICON, InterSystem Coupling-3 (ISC-3), Integrated Cluster Bus (ICB-3 and ICB-2), OSA-2, and OSA-Express channels.

1.1.3.7 Hardware Configuration for the Coupling Facility Model
The coupling facility model is a stand-alone coupling facility and is recommended for use as a production coupling facility.

The coupling facility model provides the following hardware elements:

- One Central Processor Complex (CPC)
- Integrated ICFs: 1 to 9
- Integrated SAPs: 2 SAPs assigned
- Memory:
  - 5GB minimum, 32GB maximum
  Valid memory configurations are 5GB, 6GB, 7GB, 8GB, 10GB, 12GB, 14GB, 16GB, 20GB, 24GB, 28GB, and 32GB
- Up to 15 logical partitions (LPs) are supported
- One Hardware Management Console (up to three additional optional Hardware Management Consoles are available) and two Internal Support Elements
- A Token-Ring Network Multistation Access Unit (MAU)
- A Modular cooling unit (MCU)
- Internal Battery Feature (IBF)
- Channels:
  - InterSystem Coupling-3 (ISC-3) channels:
    - 0 minimum; 32 maximum; available in increments of 1
  - Integrated Cluster Bus (ICB-3) channels:
    - 0 minimum; 16 maximum; available in increments of 1
  - Integrated Cluster Bus ICB-2 channels:
    - 0 minimum; 16 maximum; available in increments of 1
- The Channel Subsystem (CSS) for the coupling facility model consists of InterSystem Coupling-3 (ISC-3) channels and Integrated Cluster Bus (ICB-3 and ICB-2) channels.
1.1.4 For Earlier 9672/9674/2003/3000/7060 Models

EC H25126 will be applied to the Hardware Management Consoles on all new builds and available as an upgrade to the Hardware Management Consoles on the following models:

- S/390 Mruptise 3000 Enterprise Server
- S/390 Parallel Enterprise Server - Generations 3, 4, 5, and 6
- S/390 Coupling Facilities C01, C02, C03, C04, and C05
- S/390 Mruptise 2000
- S/390 Application StarterPak
- S/390 Parallel Enterprise Servers - Rn1, Rn2, and Rn3 Models
- S/390 Parallel Transaction Servers - E0n and P0n Models

EC H25126 brings no new function or functional enhancements to these models.

1.1.5 The zSeries 900 Hardware System Area (HSA)

The Hardware System Area (HSA) contains the CPC Licensed Internal Code (LIC) and configuration dependent control blocks. HSA is not available for program use.

The HSA size varies according to:

- Power-on reset (POR) mode of the CPC
- Number of installed CP’s and SAP’s
- Size and complexity of the system I/O configuration

**Note:** The zSeries 900 models support 512K HSA subchannels with a 63K per image limit for LPAR mode. The subchannel capabilities affect HSA storage requirements to accommodate the associated configuration tables.

- Whether or not dynamic I/O configuration is enabled

  **Note:** Because of the 512K HSA subchannel capability, using a large expansion percentage will have an additional impact on the HSA size.

- Whether or not concurrent LIC patches are authorized

**HSA Size Notes:**

1. When counting channels without dynamic I/O enabled, count the number of channels defined in the IOCDS, not the number of installed channels. With dynamic I/O enabled, HSA is allocated assuming maximum (256) channels.

2. To determine the number of HSA subchannels, refer to the IYP IOCP IODEVICE report under the **HSA Total** column for Subchannels. If you use HCD, you can find the total number of HSA subchannels in the Device Detail report.

   If dynamic I/O configuration is enabled, apply the expansion factors you specified on the Dynamic I/O Options panel in the current Reset profile.

Some amount of installed central storage is reserved for the HSA to hold processor Licensed Internal Code (LIC). When you initially define the amount of central storage to allocate to your partitions, it is recommended that you assume that a maximum amount of 256 MB or 384 MB is required for the HSA. Select 256 MB if your memory is \( \leq 32768 \) MB. Select 384 MB if your memory is \( > 32768 \) MB.
**Basic Mode HSA Allocation for general purpose models’ CPCs**

For general purpose models’ CPCs for Basic mode, plan for a maximum of 128 MB for HSA.

If your CPC is in Basic mode and dynamic I/O configuration changes are enabled, your HSA size includes 4 to 6 MB for coupling facility, depending on the installed storage. If your CPC is in Basic mode and dynamic I/O configuration changes are **NOT** enabled, your HSA size includes 5 MB for coupling facility if a CF channel path is defined in your IOCDS.

The HSA size required for concurrent LIC patches in Basic mode is approximately 8 MB.

The HSA granularity in Basic mode is 1 MB.

**LPAR Mode HSA Allocation for General Purpose Models’ CPCs**

When you initially define the amount of central storage to allocate to your partitions, it is recommended that you assume that a maximum amount of 256 MB or 384 MB is required for the HSA.

- Select 256 MB if your memory is \( \leq 32768 \) MB.
- Select 384 MB if your memory is \( > 32768 \) MB.

If your CPC is in LPAR mode, your HSA size includes 5 MB to 25 MB for coupling facility depending on the number of logical partitions defined and on the installed storage.

The HSA size required for concurrent LIC patches in LPAR mode is approximately 10 MB.

If future additions of I/O are planned (concurrent conditioning), be sure to provide enough HSA for additional devices by specifying a large enough dynamic expansion percentage at IML, or by overgenering your IOCDS to define anticipated additions. Until dynamic I/O support for peer coupling channels is available (3Q01), overgenering should be exploited for peer coupling channels.

The HSA Granularity in LPAR mode depends on the memory increment size. See the *zSeries 900 System Overview*, SA22-1027, for details on HSA granularity.

1.1.6 Miscellaneous Lower Level ECs included in CPC System Code EC H25128 with HMC System Code EC H25126

Following is a list of miscellaneous changes included in CPC system code EC H25128 with HMC system code EC H25126:

<table>
<thead>
<tr>
<th>EC Number</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>H25080</td>
<td>Backup-DVD New Build &amp; MES Upgrade</td>
</tr>
<tr>
<td>H25079</td>
<td>SUL-DVD 3X Drivers</td>
</tr>
<tr>
<td>H25078</td>
<td>Security-Log DVD</td>
</tr>
</tbody>
</table>
Table 1-2 (Page 2 of 2). Miscellaneous ECs in Driver 36H

<table>
<thead>
<tr>
<th>EC Number</th>
<th>Name</th>
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</thead>
<tbody>
<tr>
<td>H24783</td>
<td>SE Upgrade &quot;Frame Roll&quot;</td>
</tr>
<tr>
<td>H25134</td>
<td>SE Codeload 3X for SE Upgrades</td>
</tr>
<tr>
<td>H25248</td>
<td>HMC Upgrade Diskette New Build &amp; MES</td>
</tr>
<tr>
<td>H24781</td>
<td>SEEPROM MCM/SCM Diskette</td>
</tr>
</tbody>
</table>

1.1.7 Input/Output Configuration Program (IOCP) Considerations

1.1.7.1 Standalone IYP IOCP
Stand-alone IYP IOCP Version 1 Release 1 Level 0 (1.1.0) provides support for the zSeries 900.

1.1.7.2 Software Corequisites
See the appropriate 2064DEVICE preventive service planning (PSP) bucket subset ID for APAR and PTF information for the zSeries 900 models.

<table>
<thead>
<tr>
<th>Operating System</th>
<th>Preventive Service Planning (PSP) Bucket Subset ID</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS/390</td>
<td>2064/OS390</td>
</tr>
<tr>
<td>VM</td>
<td>2064VM/ESA</td>
</tr>
<tr>
<td>VSE/ESA</td>
<td>2064VSE/ESA</td>
</tr>
</tbody>
</table>

1.1.7.3 Publications
The following edition of the IOCP publication documents the stand-alone IYP IOCP 1.1.0 release level:


1.1.8 Preventive Service Planning (PSP) Bucket Considerations
Use IBM Service Link or contact your IBM representative to obtain a current copy of the 2064DEVICE bucket applicable to your environment. The PSP bucket contains corequisite software and hardware planning information that applies to various operating system environments. This includes, for example: authorized program analysis reports (APARS), program temporary fixes (PTFs), and Licensed Internal Code (LIC) product patches.