New and Not-So-New Assembler Instructions

Instructions Your Mother Never Told You About

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Amusing Statistics

- ESA/390 was introduced with 105 general instructions
- Today ESA/390 has 160 general instructions
- z/Architecture has 280 general instructions
- Principles of Operation is approaching 1000 pages
  - Formatting is getting smaller to keep the size "manageable"
New Instructions

- New instructions are typically introduced as a "facility"
  - If a facility isn't installed, an attempt to use the instruction will receive an operation exception
- The TPF lab generally can't use new instructions in mid-release
- "Architecture level-set" is required for TPF to begin using new instructions
- Customers can use anything supported by their own machines
String-Instruction Facility

- Move String (MVST), Compare Logical String (CLST), Search String (SRST)
- These instructions allow programs to easily deal with C-format (null-terminated) strings
- These instructions handle long lengths, but are not interruptible
  - The condition code indicates when the operation is complete
Relative-and-Immediate Facility

- Immediate instructions provide a 2-byte immediate operand

- AHI, CHI, LHI, MHI, and TMH/TML

- Examples
  - AHI  R2, 4096*2
  - TMH  R15, x'0180'
  - BNZ  label
R&I Facility (cont.)

- Relative branch (Jump) instructions provide branching to locations relative to "here"
  - BRAS, BRC, BRCT, BRXH, BRXLE

- Provides a larger destination range (±64K) than base/displacement

- Operand is interpreted as signed number of halfwords relative to the current instruction address
Can be used to eliminate base registers from code

- A register is still needed to refer to local constants, work areas, etc.

Coded like normal branch instructions; the assembler figures out how to assemble it.

- \[ \text{JNE NEXT} \rightarrow A774 \text{ 000A} \]
  \[ \text{DC XL16} \]
  \[ \text{NEXT DS 0H} \]

Very useful for branching to and writing patch code
This facility also provided Multiply Single (MS, MSR) instructions

- No requirement for an even-odd pair
- No waste of a register for a product known to require only 32 bits

These instructions were the start of 3-digit opcodes

- Decoding instructions is more complicated
- Example:
  - LHI opcode is A7x8
  - LHI 4,−256 --> A748 FF00
Compare-and-Move-Extended

- Provides CLCLE and MVCLE instructions
- Operand lengths can be up to 2G-1
- Eliminates all of those move and compare loops that only worked with 16M at a time(!).
Checksum Facility

- Uses a single instruction to perform a common algorithm

- Old way:
  * R1 = checksum
  * R2 = operand address
  * R3 = operand length

  ```
  SRL R3,2  ; Convert to fullwords
  LTR R3,R3 ; Is length zero?
  BZ DONE   ; Yes - checksum in R1
  LOOP
  DS 0H
  AL R1,0(,R2) ; Add next 4 bytes
  BC CC0+CC1,NOCARRY ; Skip if no carry
  AL R1,=F'1' ; Add the carry
  NOCARRY
  DS 0H
  AHI R2,4 ; Skip to next fullword
  BCT R3,LOOP ; Continue, if more
  DONE
  DS 0H
  ```
New way:

```
LOOP    DS    0H
CKSM    R1,R2  Calculate checksum
BC      CC3,LOOP  Repeat until finished
```
Perform Locked Operation

- Highly complex instruction that provides multiple operations under control of a lock
  - Compare and Load
  - Compare and Swap
  - Double Compare and Swap
  - Compare and Swap and Store
  - Compare and Swap and Double Store
  - Compare and Swap and Triple Store
Floating-Point Extensions

- 12 new floating-point registers (total of 16)

- New BFP format, which allows for IEEE floating-point conformance

- Extensions to existing HFP format to provide compatibility with BFP format
Extended-TOD-Clock Facility

- Provides a 16-byte TOD clock
- Adds 5 lower-order bytes of extra resolution
- Adds 1 high-order byte for rollover in September of 2042
- Adds 2 lowest-order bytes to contain user-programmable data
  - Data is retrieved from the CPU-unique TOD programmable register
  - Can be used to provide cross-system uniqueness
Store System Information

- Allows a program to obtain information about the real machine, LPAR, and virtual machine
  - Manufacturer
  - Machine type and model
  - CPU count
  - CPU capability factors
  - Partition name, VM userid name
  - Etc.
Extended-Translation 1

- Unicode / UTF-8 conversions
- Translate Extended can replace a Translate and Test that is used to find the end of a string, followed by a Translate that is used to translate the string (e.g., null-terminated strings)
Retrofits from z/Architecture

- Add Logical With Carry (ALC, ALCR), Subtract Logical With Borrow (SLB, SLBR)
  - Allow more efficient 64-bit addition and subtraction
- Long operands (BRASL, BRCL, LARL)
  - Use a 32-bit signed number of halfwords
  - Destination range of ±4G from current instruction
- Multiply/Divide Logical (ML, MLR, DL, DLR)
  - Use 32- and 64-bit unsigned operands
Retrofits (cont.)

- Extract PSW
  - Stores the current PSW contents in a register
- Load Reversed (LRV, LRVR, LRVH), Store Reversed (STRV, STRVH)
  - Can convert big-endian data to little-endian data and vice versa
- Rotate Left Single Logical
  - Similar to Shift, but bits reappear at the other end
- Set Addressing Mode (SAM24, SAM31), Test Addressing Mode (TAM)
Extended-Translation 2

- ASCII Pack and Unpack
- Unicode Pack and Unpack
- Unicode Move and Compare Logical
- Translates
  - 1 to 1
  - 1 to 2
  - 2 to 1
  - 2 to 2
All old (32-bit) instructions are still supported.

Similar instructions with 64-bit operands have a "G" in the mnemonic.
► For example, LG

Similar instructions with 64- and 32-bit operands have a "GF" in the mnemonic.
► For example, LGF

The number of variations of some instructions is large.
Examples:

- **Add:** A, AG, AGF, AR, AGR, AGFR, AH, AHI, AGHI, AL, ALG, ALGF, ALR, ALGR, ALGFR, ALC, ALCG, ALCR, ALCGR
- **Load:** L, LG, LGF, LR, LGR, LGFR, LH, LHI, LGH, LGHI, LLGF, LLGFR, LLGH, LLGC, LLGT, LLGTR, LLIHH, LLIHL, LLILH, LLILL
New z/Architecture Instructions

- Immediate instructions to operate on each halfword of a register
  - And Immediate (NIHH, NIHL, NILH, NILL)
  - Insert Immediate (IIHH, IIHL, IILH, IILL)
  - Load Logical Immediate (LLIHHH, LLIHL, LLILH, LLILL)
  - Or Immediate (OIHH, OIHL, OILH, OILL)
  - Test Under Mask (TMHHH, TMHL)
- Load Logical, Load Logical Halfword, Load Logical Character, Load Logical Immediate
New z/Arch Instructions (cont.)

- Load Pair from Quadword
  - Provides quadword consistency
Store Facility List

- Executed by the operating system at IPL time
- Stores a bitmap of facilities available on the CPU
- Bitmap can be accessed by any application program to determine if an instruction can be used
- "Chicken-and-egg" problem on ESA/390 systems
Facility Summary

- String-Instruction Facility (6/92)
- Immediate-and-Relative-Instruction Facility (9/96)
- Compare-and-Move-Extended Facility (9/96)
- Checksum Facility (9/96)
- Perform-Locked-Operation Facility (6/97)
- Floating-Point Extensions (5/98)
- Extended-TOD-Clock Facility (8/98)
- Store-System-Information Facility (1/99)
Facility Summary (cont.)

- Extended-Translation Facility 1 (4/99)
- z/Architecture Retrofits (10/2000)
- Extended-Translation Facility 2 (10/2000)